Line-End Shortening is Not Always a Failure

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ABSTRACT

Line-end shortening (LES) has always been considered a catastrophic failure in circuits. However, we find that a device with some LES can continue to function correctly. Such devices have large drive current and reduced capacitance at the expense of much higher leakage current. In this paper, we investigate the power and performance characteristics of devices with LES. Our simulations show that LES does not always cause catastrophic failure of device functionality. However, in this regime LES can lead to parametric failures, aspects of which we investigate .

Categories and Subject Descriptors:
B.8.1 [Hardware]: Performance and Reliability – *Reliability, Testing and Fault Tolerance*
General Terms: Design, Reliability
Keywords: Line-end shortening, TCAD

1. Introduction

Imperfections in lithographic printing cause shortening of the polysilicon gate in MOS devices. Line-end shortening (LES) [1] is considered a catastrophic failure that renders devices useless. To prevent this, considerable line end extension is applied at the expense of cell area. In this paper, we observe that in spite of LES, a device *can* function correctly. Devices with LES are extremely fast and leaky, with lower capacitance than the non-LES devices. We construct an equivalent circuit model for LES devices and analyze the voltage-transfer curves as well as stage delays for inverters. Using a canonical circuit, we show change in delay and power when LES occurs. In the end, we propose a smarter parametric method to filter tolerable LES failures.

2. TCAD Simulation Structure

To analyze the effect of line-end shortening on the drive strength and the subthreshold leakage of a device, we use 3D TCAD simulation (DaVinci) [2]. We try to match our device characteristics to an industrial 90nm technology. The device structure we use for analysis is shown in Figure 1. The device has a physical gate length of 70nm. NMOS device width is 400nm and PMOS width is 800nm. We sweep the LES from 0 to 50nm at the top edge to quantify the Ion and Ioff variation from the nominal device. The nominal device has 100nm line end extension from the active edge. The device is surrounded by Shallow Trench Isolation regions to check lateral current flow.

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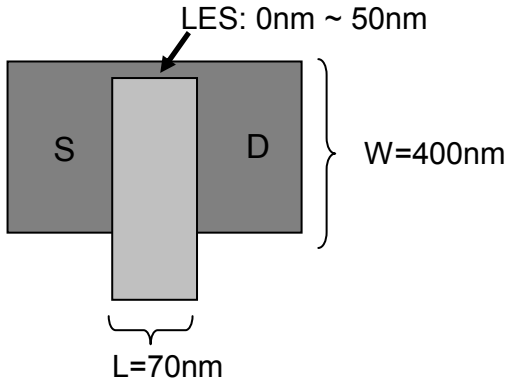
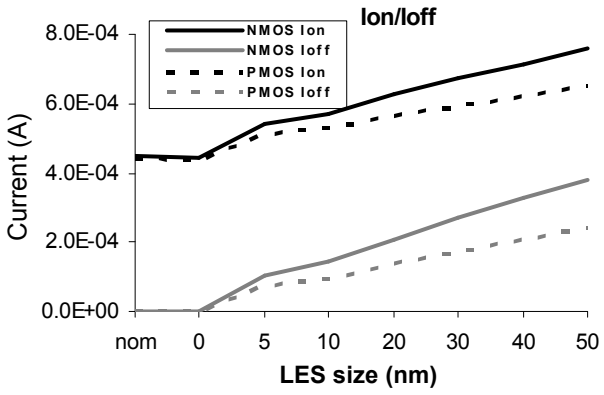
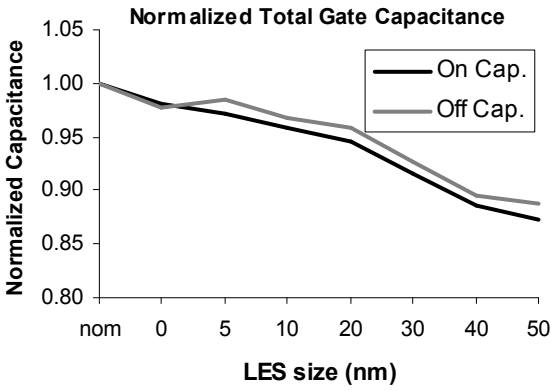


Figure 1. Device structure for TCAD simulations.



(a)



(b)

Figure 2. Ion/Ioff current in NMOS and PMOS devices (a) and normalized gate capacitance (b) with LES.

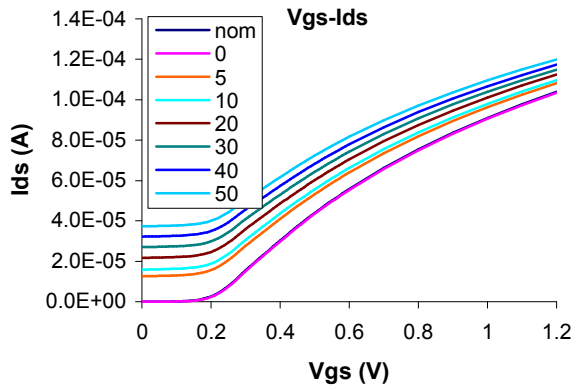


Figure 3. Id-Vgs characteristics of LES devices (NMOS).

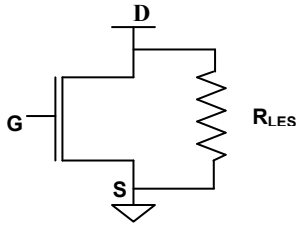


Figure 4. Equivalent circuit model for the LES device.

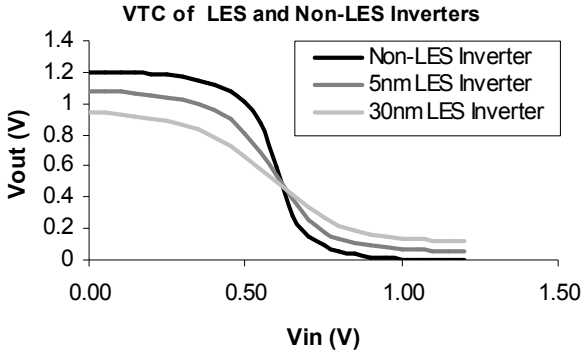


Figure 5. Voltage transfer characteristics of LES and non-LES inverters.

Figure 2 shows the drive current and subthreshold current change for NMOS and PMOS (a) and total gate capacitance change in NMOS (b) as the line-end shortening increases. As can be seen from the figure, Ion increase from small shortening (e.g., 5nm) is more than 20% in NMOS and 17% in PMOS; this is at the expense of Ioff. Total gate capacitance decreases with LES size by 3% (at 5nm) to 13% (at 50nm). As Ioff increases by three orders of magnitude, this tradeoff is generally not a desirable one. This is further clarified in Figure 3, which shows the gate characteristics of the line-end shortened devices. However, in the next section, we show that the functional correctness of a circuit can still be maintained.

3. Circuit Perspective on LES

Figure 4 shows the equivalent circuit model for an LES device. The value of R_{LES} depends on doping as well as on the width of the LES portion. Figure 5 compares the voltage transfer characteristics of an inverter with and without LES. The output voltage range is from 56mV to 1.08V. This gives a maximum Vgs of 120mV, which is far below the typical threshold voltage; therefore, no device in the following stages is accidentally turned on. This inverter has both N and P devices with LES. Similar experiments can be performed for only N or only P LES. It is important to note that the increased Vgs increases the leakage of the subsequent stage and may cause parametric failures.

Table 1. V-Swing Degradation in Canonical Circuit

LES (nm)	VDD (mV)
Nominal	0.05
0	0.05
5	1.04
10	3.20
20	7.50
30	13.30

Table 2. Delay of Canonical Circuit for LES Structures

Structure	Rise(ps)	Fall(ps)
Nominal	25.59	26.11
5nm Symmetrical	25.30	25.79
5nm PMOS Only	22.60	27.06
5nm NMOS Only	27.26	23.22

We create a canonical circuit consisting of an LES inverter surrounded by two regular inverters, and observe that LES is not a functional failure for all practical values. Table 1 gives the Vdd degradation at the output of the third inverter and Table 2 shows the impact on circuit delay. When both NMOS and PMOS are LES, the short-circuit current reduces the impact of increased Ion. However there is significant speedup when only one device is LES. It is necessary to verify potential hold-time failures due to the speedup. The worst-case LES-dependent delay improvement can be derived from process tolerances (misalignment and lithographic line-end pullback). In summary, interaction of parametric failures with LES is as follows.

1. Practically reasonable values of LES will not cause functional failure of the device.
2. LES is unlikely to cause parametric failures in setup-critical paths.
3. Hold-time critical devices should be carefully checked for LES.
4. Though LES will not always cause failure in clock paths, it is safer to not have LES on clock paths.

4. Conclusions and Future Work

We show that line-end shortening is not always a failure. We also show that under most circuit conditions, line-end shortening does not catastrophically affect circuit functionality. We have studied simple canonical circuits to assess performance impact of LES, and conclude that LES leads to faster devices which still function but with less than rail-to-rail swing. We are currently pursuing further investigations of LES phenomena and tying the results up into a design-aware smart lithography rule checker.

5. REFERENCES

[1] X. Shi et al., "Experimental Study of Line End Shortening", *Proc. SPIE*, 1999.

[2] Davinci User's Guide, Version X-2005.10-0, October 2005, http://www.synopsys.com