Modeling Edge Placement Error Distribution in Standard Cell Library

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ABSTRACT

In this work we present a predictive model for the edge placement error (EPE) distribution of devices in standard library cells based on lithography simulations of selective test patterns. Poly-silicon linewidth variation in the sub-100nm technology nodes is a major source of transistor performance variation (e.g., Ion and Ioff) and circuit parametric yield. It has been reported that significant part of the observed variation is systematically impacted by the neighboring layout pattern within optical proximity. Design optimization should account for this variation in order to maximize the performance and manufacturability of chip designs.

We focus our analysis on standard library cells. In the past the EPE characterization was done on simple line array structures. However, the real circuit contexts are much more complex. Standard library cells offer a nice balance of usability by the designers and modeling complexity. We first construct a set of canonical test structures to perform lithography simulations using various OPC parameters and under various focus and exposure conditions. We then analyze the simulated printed image and capture the layout-dependent characteristics of the EPE distribution. Subsequently, our model estimates the EPE distribution of library cells based on their layout. In contrast to a straight-forward simulation of the library cells themselves, this approach is computationally less expensive. In addition the model can be used to predict the EPE distribution of any library cells and not limited to those that are simulated. Also, since the model encapsulates the details of lithography, it is easier for designers to integrate into design flow.

Keywords: standard cells, EPE, lithography simulation, modeling

1. INTRODUCTION

OPC is effective in achieving linewidth control if optical conditions during lithography match the simulated optical conditions used to arrive at the OPC solution. Defocus and exposure dose variations result in linewidth variation even after OPC. Focus variation during lithography is caused by changes in resist thickness, wafer topography and relative distance between wafer plane and the lens system. The dose variation typically comes from the scanner or from the illumination in the optical lithography system. Depth of focus and exposure latitude define the process window of a lithography system. Latest advances in process window aware OPC[1] guarantee acceptable lithography quality but linewidth still varies within the process window. Linewidth variation has a direct impact on timing and leakage of designs. Timing sign-off prior to tapeout is no longer valid because of linewidth variation.[11] Simulation of lithography process on a circuit at different defocus, exposure and etch conditions yields its critical dimensions in silicon. Timing analysis based on circuit delay models constructed from post-lithography critical dimensions can enable designers perform robust optimizations that are tolerant to variation. Increasing stand-by leakage current is a growing concern for designers. Stand-by leakage has an exponential dependence on linewidth. Small changes in linewidth translate to exponential changes in leakage power. Evaluation of leakage behavior of designs in silicon is critical for reducing leakage power. Analysis of residual CD error after OPC and lithography simulation (litho-sim) can be used to analyze the impact of parameters such as defocus, exposure dose on performance and leakage.

Full-chip litho-sim for evaluating linewidths is extremely time consuming as it involves convolution operations between an optical kernel and layout. For standard cell-based layouts, full-chip post-litho linewidth evaluation

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can be speeded up by running litho-sim on individual standard cells and then accounting for the variation in linewidth due to the presence of other cells in a layout placement context. This technique referred to as library-based litho-sim has been reported in[4] and.[11] Though library-based litho-sim approaches are simple to implement, they do not offer any insight into the systematic variation of linewidth with changing imaging and exposure conditions. In addition to linewidth variation, printability of features below 100nm is the source of other problems such as contact misalignment, bridging and necking faults, that impact yield directly. To characterize the interactions between pattern layout and its printability, a sound understanding of impact of litho parameters on layout is required. In this work we attempt to address this topic. We propose to model linewidth variation of polysilicon (poly) patterns in standard cells in terms of imaging and exposure parameters. We first model the linewidth variation of test patterns that capture the interaction between poly patterns within and across standard cells. Based on the trends observed from test patterns, we propose to *predict* linewidth variation of poly patterns at different imaging and exposure parameters. Layout analysis based prediction of systematic variation can be used for constructing pattern-dependent timing and leakage libraries, which further can be used for design optimization.

This paper is organized as follows. In Section 2 we present our methodology for prediction of device EPEs in standard cells in detail. In Section 3 we describe EPE trends of test patterns across process window in detail and describe statistical model construction. The methodology for prediction of device EPEs in standard cells is presented in Section 4. We summarize the contributions of this work and present future directions in Section 5.

2. MODELING SYSTEMATIC EPE

Through-focus linewidth variation is partly systematic and this cannot be corrected by OPC. Though SRAF reduces the impact of focus on linewidth, it is still a source of leakage and its variability. Several recent works[2, 3, 6–8, 10] have characterized the impact of focus and exposure dose variation on linewidth. However, this class of work addresses linewidth variation of line-and-space (L/S) patterns which are not representative of poly layout in standard cells. It is well-known that OPC models tuned for L/S patterns fail to provide good coverage of optical affects leading to linewidth variation, corner rounding and line-end shortening. Hence, we characterize the behavior of test patterns representative of poly in standard cells. Although the underlying behavior of the proposed test patterns with focus and exposure is similar to that of L/S patterns, we observe that there is a systematic layout-dependent component of variation. Note that the goal of this work is to model the variation of gate length of devices only. We model the impact of focus and exposure *after OPC*. The increase in complexity of a layout during OPC changes according to OPC flags (number of iterations, step size, site definitions etc.), fragmentation and corner correction parameters. Since modeling OPC itself is complicated and impractical, we model the impact of OPC on residual linewidth error after lithography. A flowchart of proposed EPE modeling method is shown in Figure 1.

2.1. Test Pattern Selection from Standard Cells

Poly in standard cell have been optimized for area, timing and power over several technology generations. The only criterion for their manufacturability has been design rule correctness and consequently, the layout complexity increased (corners and jogs). Achieving good linewidth control is difficult with complex poly patterns and this has prompted a move towards radical design restrictions (RDR) (i.e., restricted design rules). On close observation of poly layouts in standard cells, we notice that individual poly themselves are not complex. It is the interaction between poly of different widths, orientations and corners that increases the complexity. To model the EPE behavior of gates, we choose simple poly configurations that occur in standard cells, based on manual observations. Alternately, geometric analysis of cell layouts (e.g., Roessler[9] et.al) can be used to determine the choice of poly configurations for studying EPE behavior. Test patterns are then constructed to model the interactions between the chosen configurations. Consider poly layouts of two standard cells in the $90nm$ technology of a pure-play foundry in Figure 2. Poly patterns in these cells can be decomposed into basic configurations shown in the Figure 3. To decompose poly patterns, we identify distinct simple shapes that can form a poly layout. To limit the number of combinations of test patterns as well as OPC and litho-sim runtime, it is important to minimize the number of distinct simple shapes.

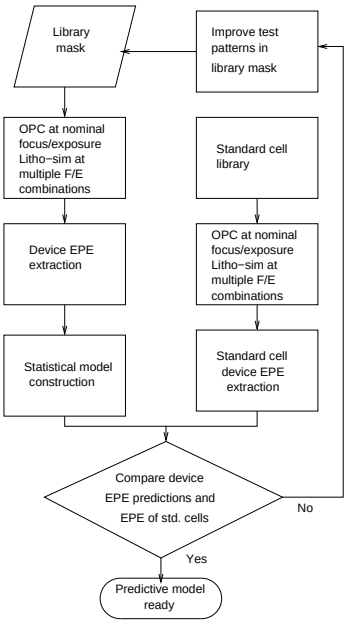


Figure 1: Predictive modeling flow for device EPE in standard cells

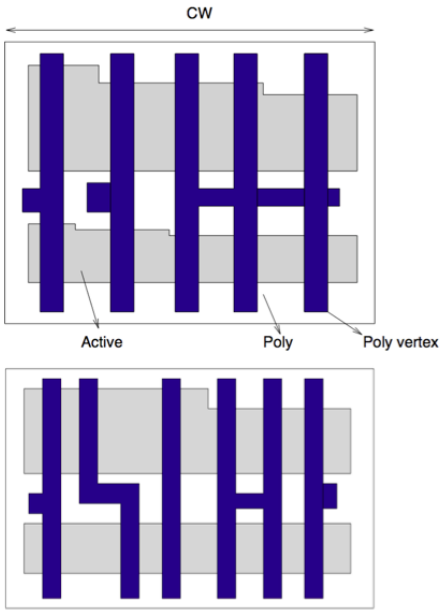


Figure 2: Typical standard cells showing diffusion and polysilicon layers

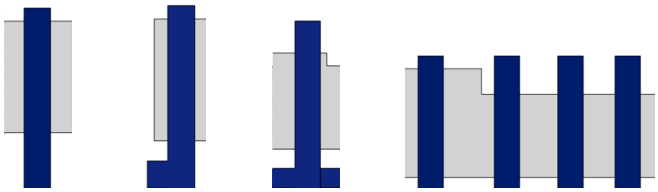


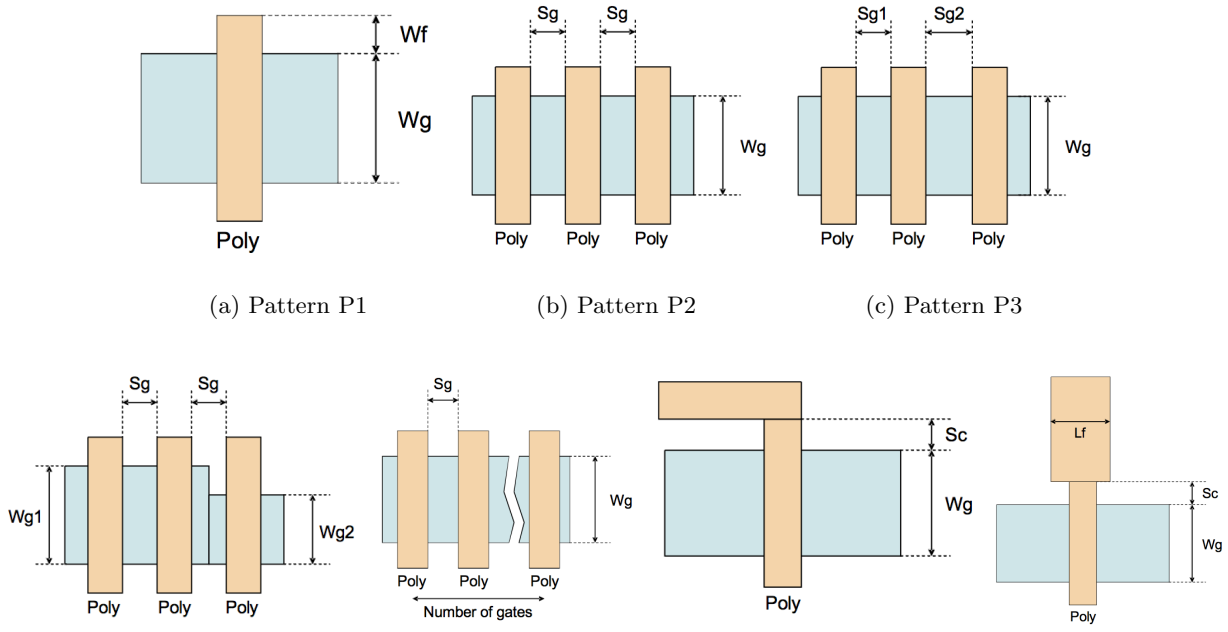
Figure 3: Poly layouts in standard cells (top row) and a possible decomposition into simple poly configurations (bottom row). Note the decomposition is not unique.

2.2. Library Mask Construction

In this section we describe the construction of test mask, referred to as the library mask, containing different configurations of simple poly patterns.

- Pattern P1: The pattern shown in Figure 4(a) investigates the relationship between device width and its EPE. In addition to width, field poly extension also determines the EPE. We vary gate width (W_g) and field poly width (W_f) and observe EPE across process window.
- Pattern P2: This pattern investigates the impact of spacing on devices of equal width in an array. The pattern shown in Figure 4(b) represents fingered poly (PMOS/NMOS) in standard cells. In addition to spacing (S_g), we vary device width (W_g) to observe the susceptibility of EPE of narrow width devices to out of focus effects.
- Pattern P3: This is an extension of Pattern P2, designed to investigate whether a linear relationship exists between device EPEs in a poly array, with varying spacings between them. A device EPE model can be made simple if the EPE of device under consideration can be deduced from EPE of other devices in the array. Figure 4(c) shows a schematic of this test pattern. We vary device width (W_g) and the spacings on each side of the gate (S_{g1} and S_{g2}).

- Pattern P4: Gate width of all devices in pattern P3 is equal. In pattern P4, we extend P3 to study the impact of different gate widths on EPE. This pattern represents edge devices of fingered poly in standard cells (refer to Figure 4(d)). We vary device width of left and right gate poly (W_{g1} and W_{g2}) and spacing between poly (S_g).
- Pattern P5: Device EPE can be impacted by the presence and the proximity of other devices beyond its immediate neighbors. This test pattern (Figure 4(e)) characterizes the interaction distance of a device with other devices. We vary the number of gates in the pattern and the spacing (S_g) between them.
- Pattern P6: Reproduction of bends and jogs is critical for linewidth control and contact alignment. A corner of field poly located near the edge of diffusion region impacts the edge placement of the gate. This impact is more pronounced at the diffusion edge of the gate where leakage current of the devices is very sensitive. This test pattern (refer to Figure 4(f)) characterizes the impact of corner distance from diffusion edge on the device EPE. We vary device width (W_g) and the spacing between the bend and diffusion edge (S_c).
- Pattern P7: Inadequate corner correction leads to large radius of curvature, resulting in large EPE at the boundary between poly and diffusion. The impact of a tapered corner is different from that of a bend. This pattern (refer to Figure 4(g) investigates the impact of distance of a tapering in poly on the device EPE. For this pattern, we vary device width (W_g), the distance between diffusion edge and wide section of tapered poly (S_c) and the width of the wide section of tapered poly (L_f).



(a) Pattern P1 (b) Pattern P2 (c) Pattern P3

(d) Pattern P4 (e) Pattern P5 (f) Pattern P6 (g) Pattern P7

Figure 4: Test patterns in the library mask

2.3. Experimental Setup

We construct library mask in the $90nm$ technology with the test patterns described in Section 2.2. Layout parameters for the test patterns are determined from poly design rules. To run OPC we construct optical model with parameters shown in Table 1. To run litho-sim, we construct aerial image models at $-100, 100, 200, 250nm$

defocus levels. OPC recipes are tuned for nominal focus/exposure conditions such that there is no residual OPC error. To generate litho simulated library mask, we run OPC at nominal defocus condition and perform litho simulation at different combinations of defocus(5) and exposure dose(3) conditions using Mentor Graphics Calibre. We do not perform assist feature insertion in this work as it introduces periodicity in variation of EPE.

3. STATISTICAL ANALYSIS OF EPE

EPE of gate poly varies along the width of the gate. There is a systematic component of the EPE variation along the device width in addition to line-edge roughness that results from resist processing. This work focuses only on the systematic component of variation due to defocus/exposure dose variation that can be studied by aerial image simulation. To observe EPE variation, we sample EPE at the top, center and bottom of the gate poly along its width (refer to Figure 5). To model and predict gate shape exactly, the number of samples can be increased. Device EPEs (EPE_{top}, EPE_{center} and EPE_{bottom}) corresponding to each pattern in the library mask are extracted using automated layout analysis programs. In the rest of this section we describe EPE trends of patterns in library mask and analyze the contributions of different layout parameters on linewidth variation at multiple defocus and exposure conditions and give statistical model for each.

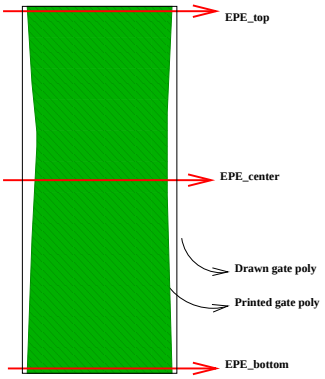


Figure 5: EPE sampling points on gate poly

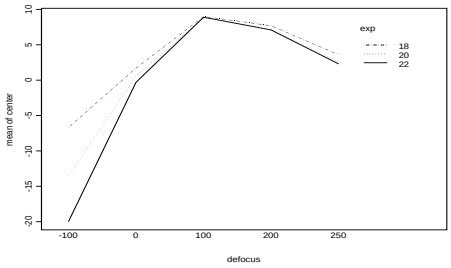
λ	0.193
NA	0.68
σ_1, σ_2	0.85, 0.57
Defocus	-0.135
Illumination	Annular
Reference threshold	0.21

Table 1: Optical model parameters.

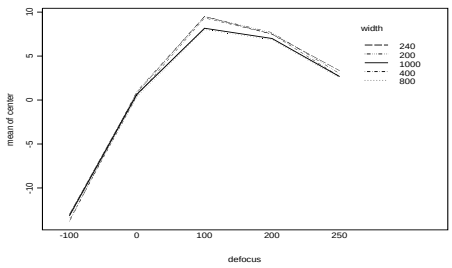
Pattern P1: The trend in EPE_{center} of pattern P1 is similar to that of an isolated line. EPE variation with focus for different exposure doses for this pattern resembles the Bossung "frown" plot as shown in Figure 6(a). EPE_{center} as a function of gate width is shown in Figure 6(b). From the plot, we can observe that EPE at the center of the device doesn't change with defocus. However, this is not correct for devices with width comparable to the gate length of the device. We also observe that field poly extension does not have any impact on EPE_{center} across different defocus conditions. Figures 6(c) and 6(d) show the trends in EPE_{center} with exposure dose for different gate widths and field poly extensions respectively. The variation in EPE is linear with exposure dose change but is practically invariant with gate width and field poly extension. However, for large values of gate width ($>$ 800nm), EPE becomes nonlinear with exposure dose. EPE_{top} and EPE_{bottom} display a similar trend with defocus and exposure dose. However, for small values of field poly extension, CD at top and bottom are more susceptible to defocus. We run linear regression to fit EPE_{center} as a function of defocus (d), exposure (e), gate width (w) and field extension (e). The functional form of the fit for our experimental setup is given by Equation 1. Plots of fit and residue for EPE_{center} with the model are shown in Figure 10. The square root of absolute errors of the fit are within $2nm$.

$$EPE_{center} = -14d^3e^2 + 54d^2e^2 - 72de^2 + 57d^3e - 257d^2e + 331de + 4e^2 - 17e - 6d^3 - 102d^2 + 119d - 0.00015w + 0.0015e + 0.086 \quad (1)$$

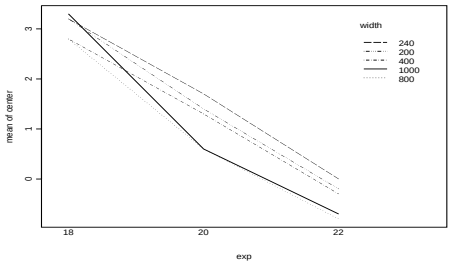
Pattern P2: EPE_{center} trend of pattern P2 across defocus and exposure dose ranges is shown in Figure 7(a). Note that the curve starts relatively flat for exposure dose corresponding to 18 (nominal value is 20) and then assumes a frown beyond nominal defocus. This is in contrast to EPE_{bottom} trend (similar to EPE_{top} trend) for the same device width and spacing. Figure 7(b) shows the EPE_{bottom} trend and we can observe that device bottom is frowning across all defocus values. At non-nominal defocus, EPE_{center} is consistently higher ("smiling") than EPE_{bottom} (or EPE_{top}) ("frowning") across different gate spacings and this trend



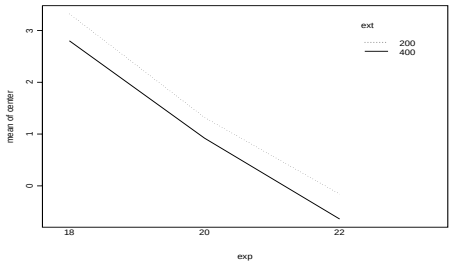
(a) EPE_{center} trend across process window



(b) EPE_{center} variation with defocus for different gate poly widths



(c) EPE_{center} variation with exposure dose for different gate poly widths



(d) EPE_{center} variation with exposure dose for different field poly extensions

Figure 6: EPE_{center} trends for pattern P1

can be observed in Figures 7(c) and 7(d) respectively. EPE_{center} variation is linear with exposure and the trend remains almost consistent across different gate poly width and spacings. But for small values of spacing, EPE_{center} variation with spacing is quadratic with exposure dose as shown in Figure 7(e). This quadratic trend is more pronounced for EPE_{bottom} as shown in Figure 7(f). An interesting trend for poly array patterns is that beyond a certain value of gate width, EPE_{center} variation is independent of width and dependent only on spacing between gates. A model of EPE_{center} obtained by linear regression of defocus, exposure dose and spacing (s) is given in Equation 2. Fit and residue plots of this model are shown in Figure 11. Absolute residuals of fit for all samples of this model are within $2nm$.

$$EPE_{center} = -14d^3e^2 + 42d^2e^2 - 52de^2 + 44d^3e - 150d^2e + 200de - 6d^3 - 6d^2 + d - 0.1sd^2 + 0.1sd + 3e^2 - 13e + 0.9 \quad (2)$$

Pattern P6: The next important pattern is the poly corner/bend. Figures 8(a) and 8(b) show EPE_{center} and EPE_{top} variation across process window. EPE_{top} is the EPE at the top of the device close to the corner/bend. We can observe that it is consistently smaller than EPE_{center} across process window. Due to the increase in radius of curvature of image contour, the printed image is pulled inside the drawn image. We observe that the change in EPE with defocus is independent of gate poly width and dependent only on spacing between line corner and diffusion edge. This trend is particularly visible in EPE_{top} than in EPE_{center} (refer to Figures 8(c) and 8(d)). Variation in EPE_{center} and EPE_{top} with exposure dose for different corner spacings is shown in Figures 8(e) and 8(f) respectively. EPE varies linearly with exposure dose for all values of corner spacings. However, EPE_{top} of patterns with small values of corner spacing is very sensitive to defocus and exposure dose variation. Figures 8(g) and 8(h) show EPE_{bottom} variation with exposure dose for different gate poly widths and corner spacings respectively. Note that the trend in EPE_{bottom} across different exposure doses differs from that of pattern P1 and this shows the impact of different OPC treatments on line-ends in presence of corners.

Regression model of EPE_{top} of P6 is a function of defocus, exposure, width and spacing to corner (s_c) and is given by Equation 3.

$$EPE_{top} = d^3(0.7e^2 + 4e - 3) + d^2(26e^2 - 118e - 73) + d(-29e^2 + 152e + 84) + 24s^3 - 29s^2 + 34s - 2 \quad (3)$$

EPE trends for pattern $P7$ follow those for pattern $P6$. However, for small values of taper distance from the diffusion boundary, EPE_{top} is consistently higher than EPE_{top} of P8 across process window. Patterns P3 and P4 are designed to test whether a linear relationship exists between EPE of a device and that of its neighbors. We observe that in a dense layout (small device spacing), EPE of a device is the space-weighted average EPE of its neighbors. This observation is in line with the result by Mikasa et.al.[7] Note that the result is valid for devices in dense poly array, within the optical radius of influence. For pattern P5, we observe that the influence of devices beyond the second poly (located at minimum spacing from each other) is negligible. Note that this is an artifact of the optical model used for OPC and lithography simulation. The actual result of this experiment may vary depending on the model and the use of assist features. The observation from P5 guides how far we should look from each device to predict its EPE across the process window.

Based on the interaction plots between defocus, exposure dose and layout parameters of test patterns, we observe that all parameters are related linearly to EPE. EPE variation for all patterns (for a given combination of layout parameters) has an underlying trend that is strongly dependent on defocus and exposure dose. This trend shifts according to the interaction between layout parameters.

4. STANDARD CELL EPE PREDICTION

To predict device EPEs in a standard cell, we first analyze its layout and classify each device into one of the pattern types in the library mask. Based on the neighborhood of each device we compute its top, center and bottom EPE based on the statistical model of the pattern. Separately, we run OPC on the standard cell at nominal defocus and exposure dose, followed by litho-sim at multiple points across the process window. For each device in the cell, we extract top, center and bottom EPEs across the process window and compare them against predicted EPE from the statistical model. The first step in predicting EPE of any device in the standard cell is its neighborhood analysis. Device surroundings determine whether it is in isolated, dense or a semi-dense context (isolated on one side and dense on the other). If the device is in a dense context, we check the widths and spacing between devices and classify them into one of the pattern types $P2$, $P3$ or $P4$. To determine the number of poly lines that should be considered for evaluating device EPE, we use the result from pattern $P5$. To compute top and bottom EPEs of the device, we check for corners and tapering of the poly in any context. In this work, we classify a device as pattern $P5$ or $P6$ irrespective of its context, to determine its top and bottom EPE (we observe that neglecting the impact of context can affect top and bottom EPE prediction significantly). In the following, we describe our methodology of matching devices to patterns using a few standard cells in the TSMC $90nm$ library. We also describe some cases where patterns in the current library mask cannot explain variation of some devices in standard cells and the need for iteratively improving library mask.

Poly and diffusion layers of standard cells INVX1, NAND2X1, AND2X1 and MX2X1 (in increasing order of poly complexity) are shown in Figure 9. Consider device $M0$ in INVX1 with gate width (W_g) of $600nm$ and a field poly extension (W_f) of $160nm$. The bottom part of the device is close to a bend in the poly and the spacing between poly corner and the diffusion boundary is $120nm$. The width of the poly bend itself is $160nm$. OPC treatment received by the top and center of the device is unaffected by the poly bend. To predict EPE_{top} of this device, we use the model of EPE_{top} of isolated poly pattern $P1$. Table 2 shows a comparison between actual and predicted values of EPE_{top} (the predicted values are marked in bold font). Note that all EPE values are indicated in nm. To predict EPE_{center} of device $M0$, we use the EPE_{center} model of pattern P1. Table 3* shows a comparison of actual and predicted values of EPE_{center}. Pattern P6 clearly represents the geometry at the bottom of $M0$. Table 4 compares the actual and predicted values of EPE_{bottom}. The maximum error in prediction is $2nm$ across 12 defocus and exposure dose conditions. We now consider device $M3$ in NAND2X1 to

*EPE is predicted for combinations of $defocus = \{0, 100, 200, 250\}nm$ defocus and $expDose = \{19, 20, 21\}mJ/cm^2$. The values of defocus and exposure dose are indicated in the first row and column respectively. All EPE values are indicated in nm.

	0	100	200	250
19	2/**1**	10/**10**	8/**6**	4/**2**
20	0/**0**	10/**10**	8/**7**	2/**3**
21	0/**-2**	10/**10**	8/**7**	2/**1**

Table 2: EPE_{top} of $M0$

	0	100	200	250
19	1/**1**	9/**9**	7/**8**	3/**3**
20	0/**0**	9/**9**	7/**8**	3/**3**
21	0/**0**	9/**9**	7/**8**	3/**3**

Table 3: EPE_{center} of $M0$

	0	100	200	250
19	0/**1**	8/**8**	6/**7**	2/**3**
20	0/**0**	8/**7**	6/**6**	2/**2**
21	0/**-1**	8/**7**	6/**6**	2/**2**

Table 4: EPE_{bottom} of $M0$

predict EPE at the center and bottom of the device. $M3$ has gate width of $600nm$, corner spacing of $140nm$ and field extension of $180nm$. Additionally, $M3$ is adjacent to $M2$ (with same gate width). To predict EPE_{center} of $M3$, we imagine a virtual neighbor to the right, with the same gate width and at a distance of $> 400nm$ (From Pattern P5, we deduced that poly beyond $400nm$ have a negligible impact on device EPE). We then use EPE_{center} model of pattern P3 for EPE_{center} of $M3$. For EPE_{bottom} of $M3$, we use EPE_{top} model for pattern P6 (since $M3$ is its inverted equivalent) and the results of comparison are shown in Table 6.

	0	100	200	250
19	1/**0**	6/**6**	4/**4**	2/**1**
20	0/**-2**	5/**4**	4/**4**	1/**-1**
21	-1/**-3**	5/**4**	4/**3**	1/**-1**

Table 5: EPE_{center} of $M3$

	0	100	200	250
19	1/**1**	7/**8**	5/**6**	3/**2**
20	0/**-1**	6/**8**	5/**6**	2/**2**
21	0/**-1**	6/**7**	5/**6**	2/**2**

Table 6: EPE_{bottom} of $M3$

The cell INVX1 has shown the quality of prediction for isolated devices. We now study EPE prediction for a dense and semi-dense context. Consider devices $M1$, $M2$ and $M5$ in cell AND2X1. $M1$ is located at a minimum spacing of $150nm$ from its left neighbor $M0$ and at a spacing of $320nm$ from its right neighbor $M5$. $M2$ is located at spacings of $270nm$ and $230nm$ from its left and right neighbors. $M5$ is located $320nm$ from $M2$ and is isolated on the right. For EPE_{center} we apply the model from pattern P2 and for EPE_{top} or EPE_{bottom} we apply pattern P8. Comparison of EPE_{top} of $M1$, EPE_{center} of $M2$ and EPE_{top} of $M5$ are shown in Tables 7, 8 and 9 respectively. Poly layout in MX2X1 is more complicated than previously shown standard cells. We first

	0	100	200	250
19	2/**0**	3/**2**	2/**2**	2/**1**
20	-2/**-2**	1/**0**	0/**0**	-1/**-1**
21	-2/**-4**	0/**0**	-1/**0**	-2/**-3**

Table 7: EPE_{top} of $M1$

	0	100	200	250
19	2/**2**	4/**6**	4/**5**	3/**3**
20	0/**-1**	2/**4**	2/**3**	0/**1**
21	-2/**-2**	1/**3**	1/**2**	0/**-1**

Table 8: EPE_{center} of $M2$

	0	100	200	250
19	2/**1**	7/**9**	6/**7**	2/**3**
20	0/**-1**	7/**9**	6/**7**	2/**2**
21	0/**-1**	7/**8**	5/**7**	1/**2**

Table 9: EPE_{top} of $M5$

compare predicted and actual EPEs of three devices and explain the short comings of the current library mask. We then analyze the sources of difference between predicted and actual EPEs.

Figure 9 shows the poly layout of MX2X1. The layout shows horizontal poly toward the top left corner of the cell creating a long extension for devices $M8$ and $M9$. Device $M1$ is surrounded on both sides with the left neighbor having a large bend towards $M1$. Device $M9$ is a narrow width device (gate width = $200nm$) with a right neighbor at a distance of $260nm$. The field poly for this device extends long distance beyond the diffusion edge before taking a bend. Hence, this device is equivalent to a narrow width device with a long field extension. We observe that devices with large spacing to corner are not sensitive to defocus and exposure. This device is also part of an array since there is a neighbor to its right within the optical radius of influence. Applying EPE_{top} pattern P1 and P5, we compute predicted EPE_{top} and compare it with its actual values in Table 10. We can observe that the maximum difference between predicted and actual EPE is $\pm 2nm$. Devices $M8$ and $M9$ are characterized by poly bends close to the diffusion boundary, lying in close proximity to other devices. The devices in the neighborhood have different widths and field offsets. This makes EPE prediction for these devices complicated. Consider predicted and actual EPE_{top} of $M8$ and $M9$ in Tables 11 and 12 respectively. The correlation between actual and predicted EPE is weak and the prediction error itself is $> 4nm$.

	0	100	200	250
19	1/**0**	6/**6**	5/**5**	2/**2**
20	0/**-2**	6/**6**	4/**4**	2/**0**
21	0/**-2**	5/**5**	4/**4**	1/**0**

Table 10: EPE_{top} of $M9$

	0	100	200	250
19	2/**-4**	6/**1**	5/**0**	3/**-3**
20	0/**-8**	4/**-1**	4/**-2**	2/**-7**
21	0/**-10**	4/**-1**	4/**-3**	1/**-8**

Table 11: EPE_{top} of $M8$

	0	100	200	250
19	3/**1**	4/**8**	3/**6**	3/**2**
20	-1/**-1**	1/**8**	1/**6**	0/**2**
21	-2/**-1**	1/**7**	1/**6**	-1/**2**

Table 12: EPE_{top} of $M1$

From the results, we can observe that device corners are very sensitive to the spacing between diffusion boundary and poly bend. The presence of another poly at minimum pitch from the corner decreases the sensitivity of the corner (the device tends to behave in a "dense" fashion). We also observe that the vertical placement of a device relative to another also impacts the EPE. Although, pattern $P4$ models this impact to some extent, it does not consider shift in placement of devices of equal width. Additionally, the presence of a corner or bend perpendicular to the gate poly also impacts EPE around the center of interaction. The current library mask does not include any pattern that explores these pattern and hence limits our prediction capability. If a poly layout configuration does not have any match in the library mask, it must be enhanced and statistical model must be reconstructed for the pattern representing the configuration.

5. CONCLUSIONS

In this work we have proposed a method for construction of a statistical model of EPE for devices in standard cells. The statistical model is based on OPC and lithography simulation of a limited set of cells representative of poly layout in cells. Our current model can predict device EPEs along the width of gate poly within $\pm 2nm$. But to ensure good coverage of all standard cells, an efficient methodology for geometric analysis of poly layout is required. Our current methodology incrementally improves the library mask to achieve good coverage of cells. To predict device EPEs in standard cells efficiently, statistical model should be supplied with values of relevant layout parameters. We are currently working on incorporating automatic layout analysis into the prediction flow.

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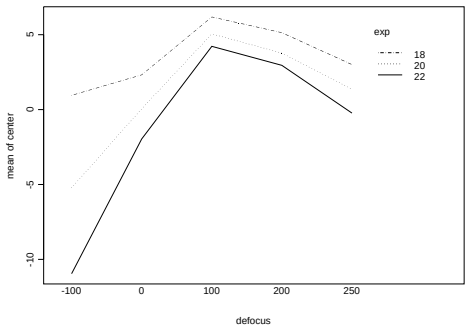
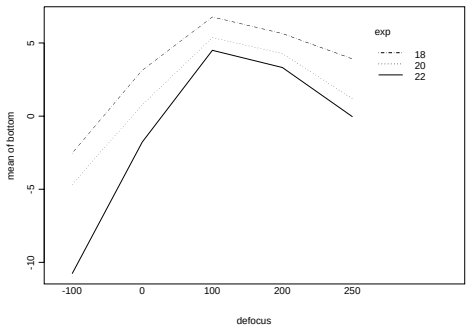
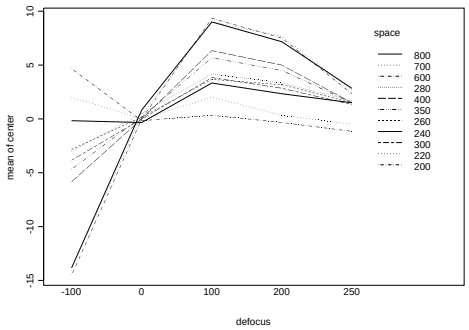


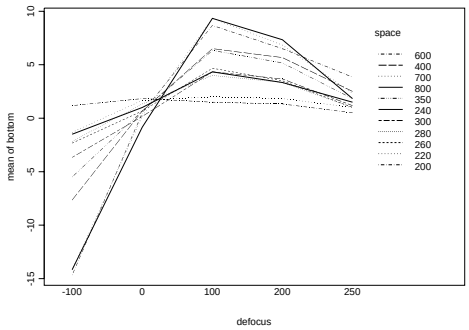
(a) EPE_{center} trend across process window



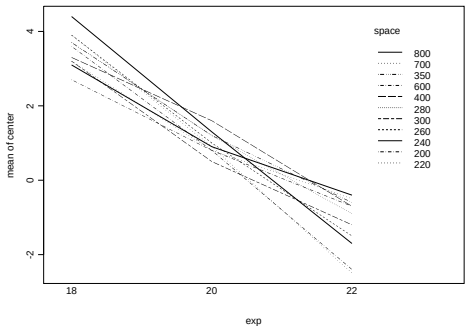
(b) EPE_{bottom} trend across process window



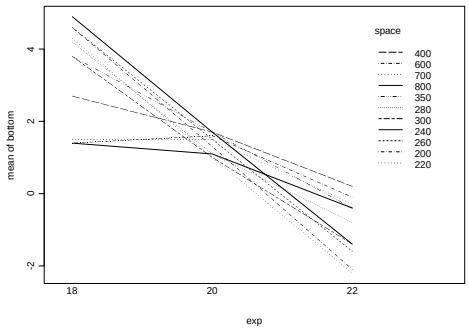
(c) EPE_{center} variation with defocus for different gate poly spacings



(d) EPE_{bottom} variation with defocus for different gate poly spacings

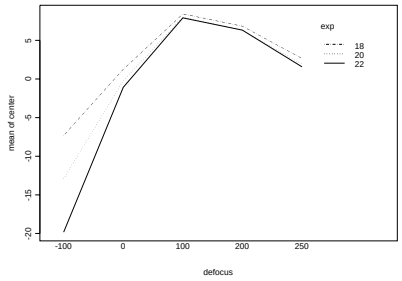


(e) EPE_{center} variation with exposure dose for different gate poly spacings

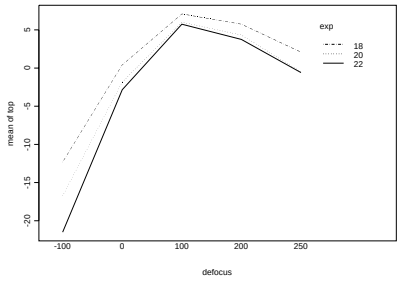


(f) EPE_{bottom} variation with exposure dose for different gate poly spacings

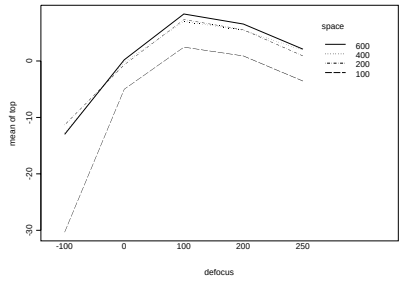
Figure 7: EPE_{center} and EPE_{bottom} trends for pattern P2



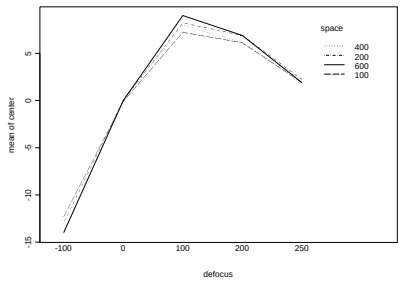
(a) EPE_{center} trend across process window



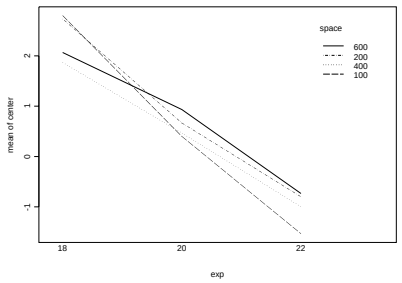
(b) EPE_{top} trend across process window



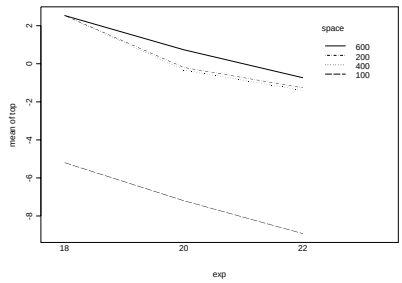
(c) EPE_{top} variation with defocus for different gate poly spacing



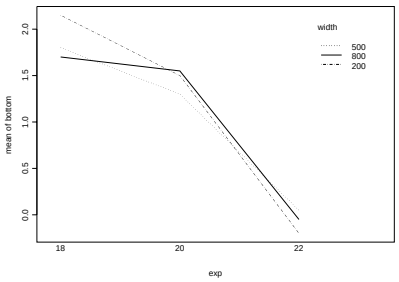
(d) EPE_{center} variation with defocus for different gate poly spacings



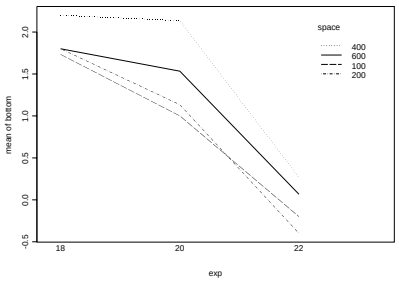
(e) EPE_{center} variation with exposure dose for different corner spacings



(f) EPE_{top} variation with exposure dose for different corner spacings



(g) EPE_{bottom} variation with exposure dose for different gate poly widths



(h) EPE_{bottom} variation with exposure dose for different gate poly spacings

Figure 8: EPE trends for pattern P6

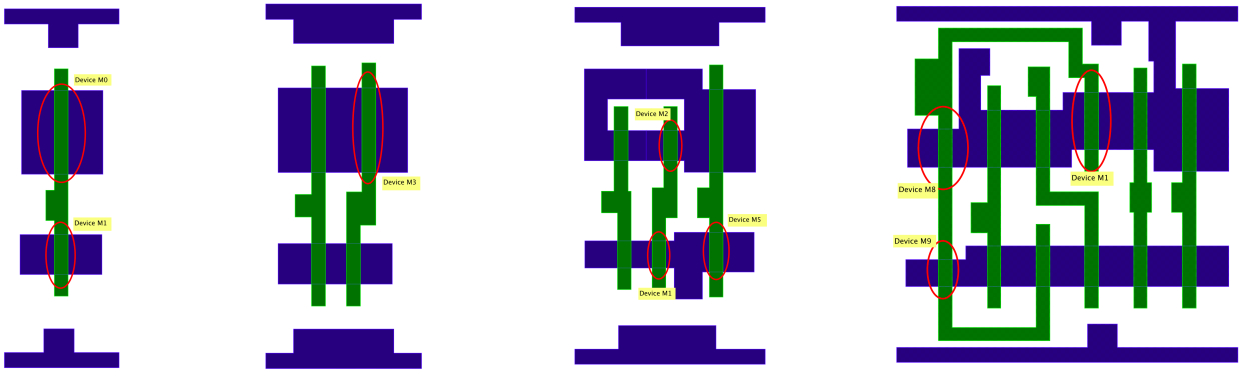


Figure 9: INVX1, NAND2X1, AND2X1 and MX2X1 in TSMC 90nm library

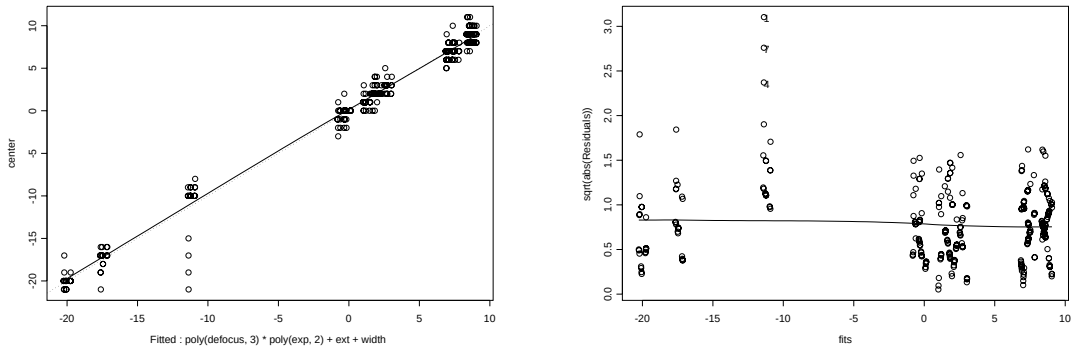


Figure 10: Fit and residue plots of EPE_{center} of P1

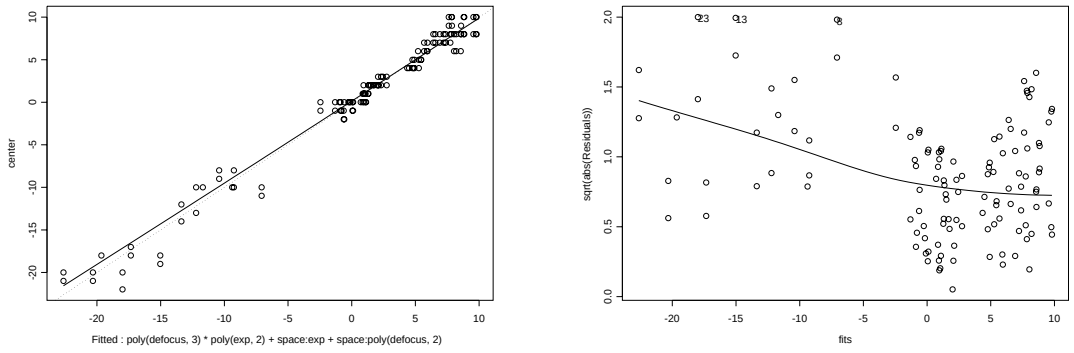


Figure 11: Fit and residue plots of EPE_{center} of P2