Modeling of Non-Uniform Device Geometries for Post-Lithography Circuit Analysis

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ABSTRACT

Current ORC and LRC tools are not connected to design in any way. They are pure shape-based functions. A wafer-shape based power and performance signoff is desirable for RET validation as well as for "closest-to-silicon" analysis. The printed images (generated by lithography simulation) are not restricted to simple rectilinear geometries. There may be other sources of such irregularities such as Line Edge Roughness (LER). For instance, a silicon image of a transistor may not be a perfect rectangle as is assumed by all current circuit analysis tools. Existing tools and device models cannot handle complicated non-rectilinear geometries.
In this paper, we present a novel technique to model non-uniform, non-rectilinear gates as equivalent perfect rectangle gates so that they can be analyzed by SPICE-like circuit analysis tools. The effect of threshold voltage variation along the width of the device is shown to be significant and is modeled accurately. Taking this effect into account, we find the current density at every point along the device and integrate it to obtain the total current. The current thus calculated is used to obtain the effective length for the equivalent rectangular device. We show that this method is much more accurate than previously proposed approaches which neglect the location dependence of the threshold voltage.

Keywords: Non-rectilinear gates, Line edge roughness, Narrow-width effect, TCAD verification

1. INTRODUCTION

For closest-to-silicon analysis, it is desired to have a wafer-shape based power and performance analysis tool. Printed images of rectilinear geometries are not restricted to rectilinear shapes. Due to Line Edge Roughness and other effects, irregularities are observed in printed shapes. A silicon image of a transistor gate is often not confined to a perfect rectangle, as is assumed by all current circuit analysis tools. These tools are unable to handle complicated geometries. Large discrepancies are observed between the simulated and observed values of circuit parameters such as current and threshold voltage.

There have been several previous approaches to modeling non-rectilinear geometries[1,2,3]. A significant drawback in all these works is that they consider the threshold voltage and hence the current density to be uniform along the device width. As a result, variations in length are treated the same, irrespective of the location of the variation along the channel.

It is known that the fringing capacitance due to Line-End Extension[6], dopant scattering due to STI edges[6], and the Well Proximity Effect (WPE)[9,10] significantly affect the device threshold voltage. These effects are more pronounced near the device edges and roll off sharply as we move towards the center of the device. The Vth and current characteristics are, therefore, different along the channel. The extent of the 'edge effect' is different for different technologies. Fig 4 shows a TCAD simulation of subthreshold current density as a function of location along the device width for a particular gate length. For this technology, it is observed that the edge current is up to 2x larger than the center current. It is important

* Part of this work was done when the author was at BLAZE-DFM, Inc. during Fall, 2005.

Design and Process Integration for Microelectronic Manufacturing IV, edited by Alfred K. K. Wong, Vivek K. Singh, Proc. of SPIE Vol. 6156, 61560U, (2006) · 0277-786X/06/$15 · doi: 10.1117/12.658087

to note that a given variation in length near the edges has a significantly different impact on the current than a variation near the center of the device. In other words, to model the effect of non-rectilinearity on gate characteristics, it is important to consider not only the dimensions of the variation, but also its location along the device width.

In this paper, we model the threshold voltage and hence the on and off current densities as functions of distance from the device edge. The coefficients of the model are empirically adjusted for different gate lengths. We use this model to analyze a non-rectilinear gate by treating it as a composition of several small rectangles of different lengths. For each rectangle, we use the current density model corresponding to its length. The total current of this rectangle is the integral of the current density over its width. The limits of the integral for a particular rectangle depend on its location, thus the value of the integral is different for each rectangle. The sum of the currents of all rectangles is the total current of the device. The total current can be used to provide an equivalent rectangular length for the device, so that it can be modeled using SPICE like tools.

The rest of the paper describes the development of our model and the simulation setup used to verify its accuracy. Section 2 provides a background and analysis of the physical effects that lead to the edge effects described above. Section 3 describes the fitting procedure used for development of the model. Section 4 describes the technology under consideration and the TCAD setup for verification of the model. Section 5 details the results from our comparisons and Section 6 concludes the paper.

2. PHYSICAL EXPLANATION OF THE EDGE EFFECT

Fig. 1 shows the cross section of a MOS device with Shallow Trench Isolation (STI) technology. To compromise the pull-back effect (i.e., line end shortening) due to defocus, certain amount of gate poly should extend over diffusion area. The extension over the STI region is defined as line-end extension.

Though the deep buried well technique has several advantages over current IC design, which include the possibility of triple-well structures and providing a low resistance path to ground for SER reduction[10], these deep buried well layers have non-negligible impact on the devices adjacent to the mask edge. Variation in the threshold voltage for those devices is observed since there is high probability for scattered ions to be implanted in the silicon surface. This effect is called the Well Proximity Effect (WPE).

All these factors contribute to the Narrow Width Effect (NWE), which is dependent on the isolation process. For non-recessed and semi-recessed (e.g., LOCOS) isolation processes, one can expect that the Vth will increase as device width decreases[5,6,11]. On the other hand, Reverse Narrow Width Effect (RNWE) in which the Vth decreases as the device width shrinks is observed in STI process[5,6,11]. The RNWE can be explained in part by the parasitic fringing capacitances (shown in Fig. 1) between gate, STI sidewall, and active area, where there is poly gate extension over the isolation area.

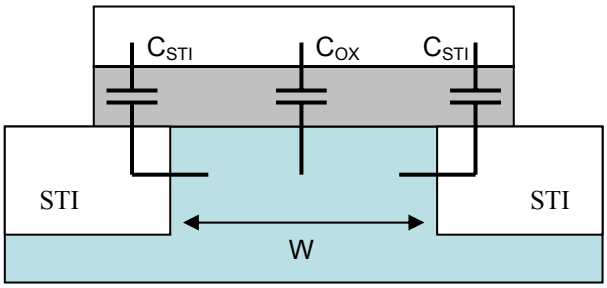

Fig. 1. Cross Section of device showing STI edges and fringing capacitances

3. DEVELOPMENT OF LOCATION DEPENDENT VTH MODEL

The solid line in Fig. 2b shows Ioff vs. Width graphs for an NMOS device for the 90nm technology under consideration. These values are generated using a TCAD setup tuned to match an industrial 90nm process closely. The device models corresponding to this industrial process are level 54 SPICE models.

The figure shows that, beyond a certain width, the current varies linearly with width, suggesting a nearly constant threshold voltage. However, as the width is decreased, the graph becomes increasingly flat till a point is reached where Ioff increases with decreasing width, which we refer to as the current 'kick-back' effect. On the other hand, the Ion curve shown in Fig 2a is nearly linear. These observations can be explained by modeling the threshold voltage as a piecewise function of location as shown in Fig 3a. The threshold voltage is constant at the center and decreases near the edges. At low widths, the effects from the two edges interact to reduce the Vth even further as shown in Fig. 3b. Ioff being an exponential function of Vth, the decrease in Vth due to width more than offsets the linear decrease in current. On the other hand, Ion is not a very strong function of Vth and thus appreciable variation in Ion is not observed. In this work, we aim to model this functional dependence by proposing a location dependent Vth model which is able to model the current 'kick-back' effect shown in the figure.

Typically, fabrication facilities do not release TCAD setups, therefore the model must be such that it can be developed entirely using SPICE data. However, in this work, we wish to verify our results against TCAD simulation. Since matching TCAD and SPICE models are not easily available, we have performed our modeling based on TCAD data. However, this data is treated *exactly* as if the values were taken from SPICE results. In other words, we use only the I vs. W characteristics to perform the fitting, which are easily obtained from SPICE simulations. TCAD data is used only for the purpose of providing a meaningful comparison point. We try to make this TCAD setup as close as possible to an industrial 90nm technology as described in Section 4.

Referring back to the Ioff vs. W plot, we note that after a width of 100nm, the current is linear with width. This suggests that for points further than 50nm from each edge, the threshold voltage is constant. However, below 100nm, the flattening of the curve indicates that this is the point where the effects from the two edges interact. We conclude that the edge effect extends to approximately 50nm on each side. This conclusion is confirmed by the Jon/Joff vs. location plot generated by TCAD simulation shown in Fig 4. The threshold voltage is thus modeled as a piecewise function of location.

We now discuss the process of determining the functional form of the threshold voltage, f(x), in the edge affected region.
The surface potential, and hence the threshold voltage at a location is a complicated function of distance from the edge.[5,11]. The Ioff density is known to be an exponential function of Vth. Since the only information available is the total current, which is the integral of the current density over the width, fitting is to be performed on this quantity. Since a function can always be approximated as a polynomial, we find the highest order polynomial whose exponential can be integrated to obtain standard functions. Mathematica[14] is able to integrate functions of the form $exp(K1*x^2+K2*x)$ conveniently. We also find that the quadratic model captures the 'kick-back' effect correctly. The functional form of the Vth is described in equations (1), (2) and (3). Where the edge effects overlap, the quadratics add up to create a stronger equivalent effect. Here, *Vth(x)* is the threshold voltage as a function of location in the edge affected region. *Vth(middle)* is the flat threshold voltage at distances beyond the edge region. The total width of the device is *W*, the width of the edge region is *w* and *K1, K2* are empirically fitted constants.

For $W >= 2w$

$$\begin{aligned} Vth(x) &= Vth(middle) - K1\times(x-w)^2 + K2\times(x-w) && 0 <= x <= w \\ Vth(x) &= Vth(middle) && w <= x <= W-w \\ Vth(x) &= Vth(middle) - K1\times(W-x-w)^2 + K2\times(W-x-w) && W-w <= x <= W \end{aligned} \quad (1)$$

For $w <= W <= 2w$

$$\begin{aligned} Vth(x) &= Vth(middle) - K1\times(x-w)^2 + K2\times(x-w) && 0 <= x <= W-w \\ Vth(x) &= Vth(middle) - K1\times(x-w)^2 + K2\times(x-w) - K1\times(W-x-w)^2 + K2\times(W-x-w) && W-w <= x <= w \\ Vth(x) &= Vth(middle) - K1\times(W-x-w)^2 + K2\times(W-x-w) && w <= x <= W \end{aligned} \quad (2)$$

For $W <= w$

$$Vth(x) = Vth(middle) - K1\times(x-w)^2 + K2\times(x-w) - K1\times(W-x-w)^2 + K2\times(W-x-w) \quad (3)$$

Figs. 3a and 3b show plots of Vth vs. location for a particular choice of *K1* and *K2* for $W >= 2w$ and $w <= W <= 2w$ respectively. The fitting is performed using Mathematica. The coefficients are adjusted to match the total current (integral of the density) to the observed values shown in Fig. 2. The procedure is repeated for different lengths and a new model is generated for each length from -10nm to +10nm around the nominal value.

When a non-rectilinear gate is encountered, it is split into several rectangles, and for each rectangle the model corresponding to its length is chosen. The limits of integration are dependent on the position of the rectangle along the width. Since the current varies along the width, integrating over different sections yields different values of total current, and the location dependence is captured.

The accuracy of the fitting model is shown for L=90nm in Fig. 2a and 2b. Although the fitting is not very accurate at low values of width (it is not possible to capture all the device parameters in this simplistic model), the trend is correctly predicted and the effective current overhead for non-rectilinear gates is still fairly accurate as discussed in the results section. It is also useful to note that the largest discrepancies are for very small values of width, which are well below the minimum sizes allowed by the process. The model behaves similarly for different values of L.

Fig 2a shows the behavior of the model for Ion. It should be noted that the Vth fit is entirely based on matching Ioff values, as this parameter is considerably more sensitive to Vth. The Ion values are calculated based on the Vth values predicted by the model.

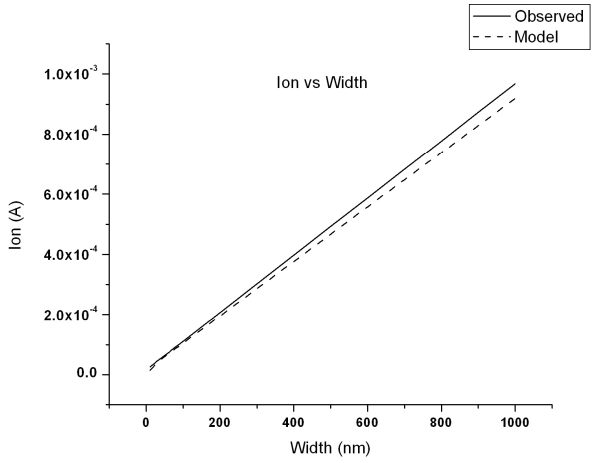

Fig 2a. Comparison of Ion vs. Width characteristics of observed data and fitted model

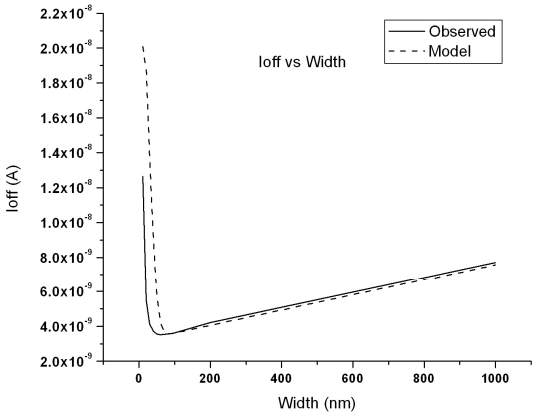

Fig. 2b. Comparison of Ioff vs. Width characteristics of observed data and fitting model

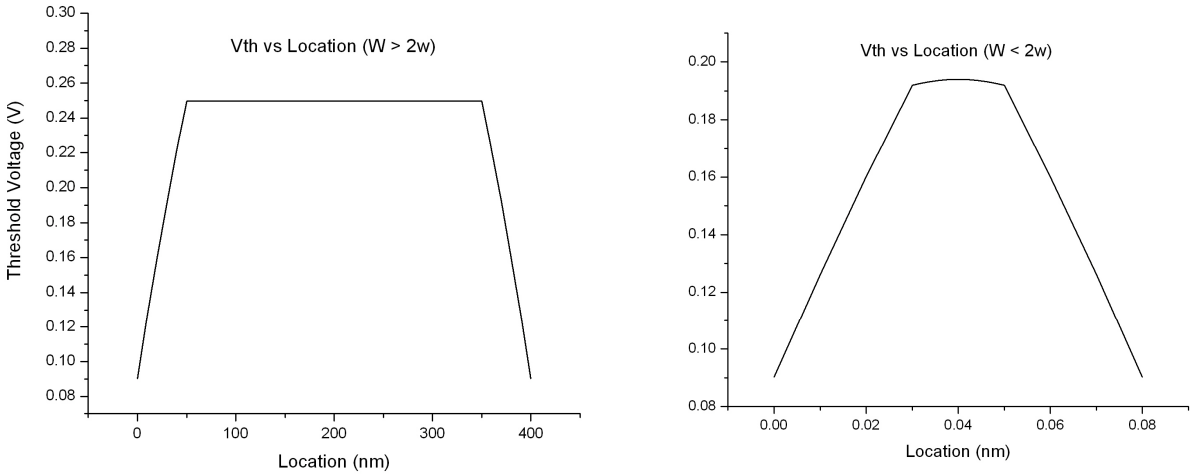

Fig 3. Vth as a function of location for a) *W >= 2w* and b) *w <= W <= 2w*

4. TCAD SETUP FOR MODEL ACCURACY VERIFICATION

To verify the accuracy of the models derived in Section 3, a 3D TCAD simulation tool Synopsys Davinci[12] is used. We generate a single N-Channel MOSFET as a baseline device with L_nominal = 90nm and Width = 400nm. To include fully-recessed oxide isolation (e.g., STI) in the simulation, we surround the devices with oxide material which is 0.1um in depth and 0.1um in width. Initial parameters of the device are taken from the ITRS 90nm technology node[13]. The values are then tuned to meet the device characteristics (i.e., Ion and Ioff) for an industrial 90nm technology obtained through SPICE simulation. The final parameters we use to measure Ion and Ioff of non-rectilinear devices are shown in Table 1. Ioff and Ion comparisons of 3D TCAD simulation results with HSPICE are shown in Fig 5. As can be seen from the plot, the discrepancy between Davinci simulation and HSPICE slightly increases as the device width increases.

Table 1. TCAD Model Parameters

Parameters	Value
L_nominal	90nm
Width	0.4um
Vdd	1.2V
Tox	1.82nm
Channel doping	3.5e+18 cm^{-3}
NSUB	3.0e+15 cm^{-3}
Junction depth	0.03um
Line-End Extension	0.1um
S/D Electrode length	0.07um
S/D Electrode width	0.4um
S/D Region to Gate poly	0.02um
STI width	0.1um
STI depth	0.1um

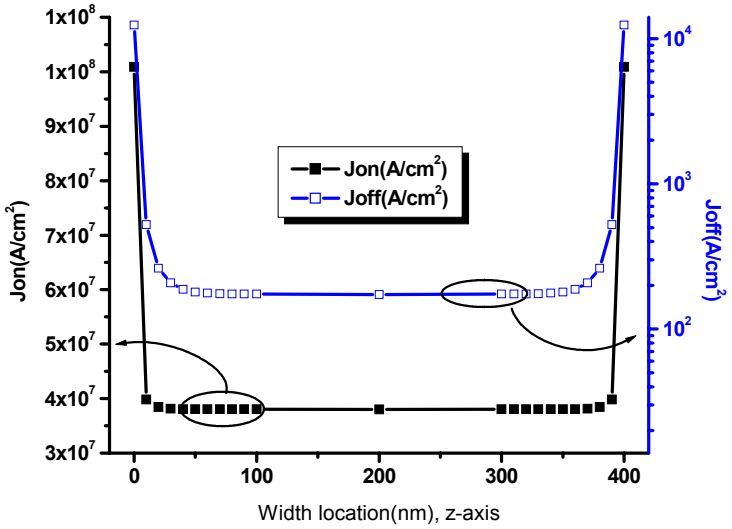

Fig. 4. On and Off current densities as a function of position along channel

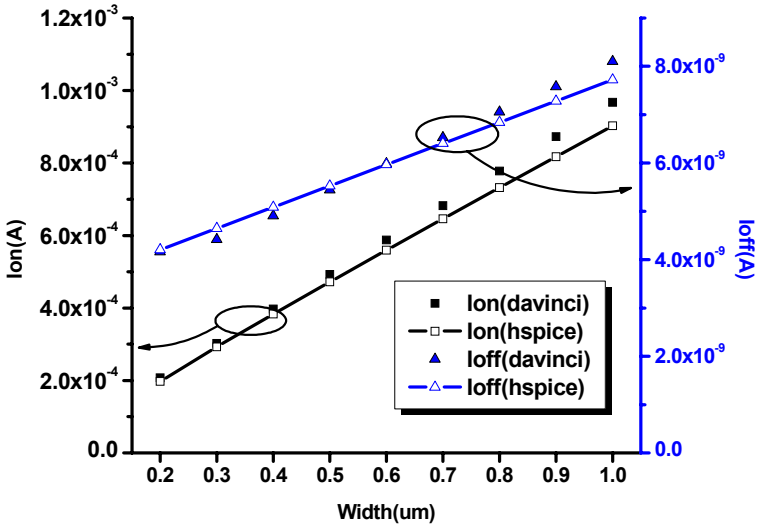

Fig. 5. Ion and Ioff as a function of width for SPICE and Davinci setups

To check the current dependency, thus Vth dependency on the location along the device width, we measure the current density along the width. Fig 4 shows the current density value along the device width (i.e., z-axis in Fig 4). As can be seen from the figure, current density along the device width represents a "tub-shaped" plot; the current through most of device is constant (i.e., flat along the z-axis) but it increases drastically over a distance approximately 50nm from device edge. These observations confirm the conclusions arrived at in Section 3.

To simulate the device performance of non-rectilinear devices we introduce an irregularity and sweep the location, width, and length of the protrusion or depression. Fig 6a shows a basic gate structure which we use for the 3D device simulation. As can be seen from the figure, $\Delta L/2$ is the half protrusion length, W' is the width of protrusion, and Z' is defined as the bottom location of the protrusion. We sweep ΔL from -10nm to +10nm with a step of 2nm, W' from 20nm to 200nm with a step of 20nm, and Z' from 0 (i.e., at the bottom edge of device) to 100nm (i.e., center of device).

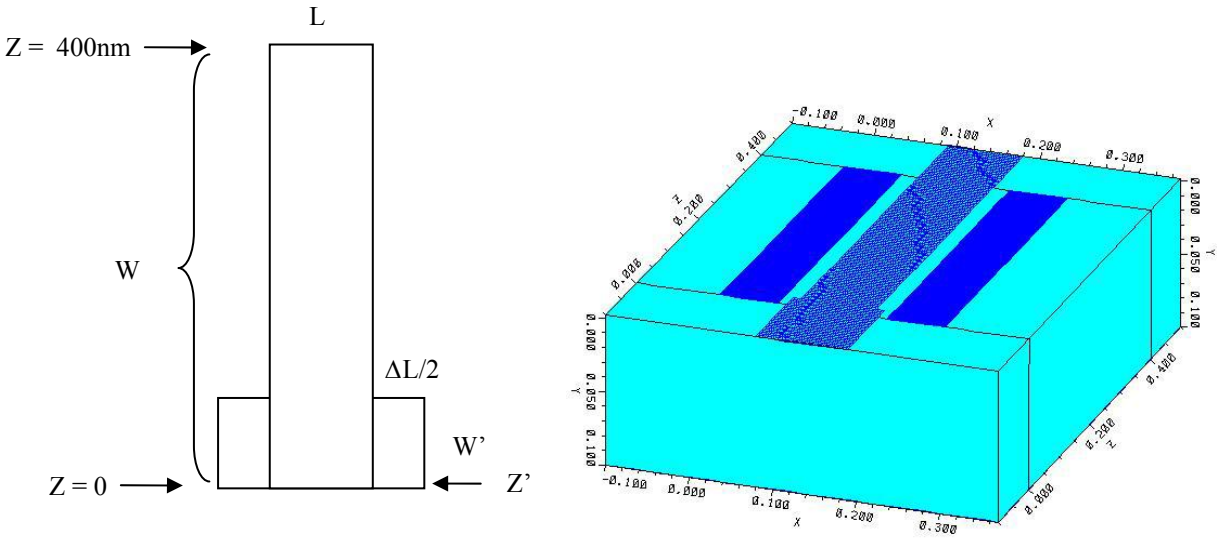

Fig. 6. Davinci structure used for verification of results a) Diagrammatic Representation : b) 3D Device Structure

Positive ΔL corresponds to a protrusion and negative ΔL corresponds to a depression. The line-end extension profile also follows the shape of the edges of devices (e.g., if there is a protrusion at the bottom edge, the length of the line-end extension is the same as the length of the protrusion). A contour plot of a 3D device mesh structure is shown in Fig 6b where ΔL/2 =+10nm, W'=20nm, and Z'=0.

5. RESULTS

Table 2. Results for non-rectilinear gates with protrusion or depression of width 20nm

Width of Protrusion/Depression = 20nm						
	Length of Protrusion/ Depression →	82	86	90	94	98
Location(nm) ↓						
0	Davinci	1.477	1.163	1.000	0.919	0.870
	Proposed Model	***1.543***	***1.194***	***1.000***	***0.911***	***0.838***
	Flat Model	1.133	1.040	1.000	0.978	0.967
20	Davinci	1.247	1.083	1.000	0.982	0.971
	Proposed Model	***1.197***	***1.061***	***1.000***	***0.970***	***0.954***
	Flat Model	1.133	1.040	1.000	0.978	0.967
40	Davinci	1.124	1.042	1.000	0.991	0.984
	Proposed Model	***1.088***	***1.024***	***1.000***	***0.989***	***0.984***
	Flat Model	1.133	1.040	1.000	0.978	0.967
60	Davinci	1.092	1.031	1.000	0.993	0.989
	Proposed Model	***1.079***	***1.021***	***1.000***	***0.991***	***0.986***
	Flat Model	1.133	1.040	1.000	0.978	0.967
80	Davinci	1.082	1.027	1.000	0.994	0.991
	Proposed Model	***1.079***	***1.021***	***1.000***	***0.991***	***0.986***
	Flat Model	1.133	1.040	1.000	0.978	0.967

Table 3. Results for non-rectilinear gates with protrusion or depression of width 40nm

Width of Protrusion/Depression = 40nm						
	Length of Protrusion/Depression →	82	86	90	94	98
Location(nm) ↓						
0	Davinci	1.660	1.217	1.000	0.880	0.800
	Proposed Model	***1.741***	***1.255***	***1.000***	***0.872***	***0.792***
	Flat Model	1.267	1.080	1.000	0.957	0.935
20	Davinci	1.340	1.111	1.000	0.961	0.930
	Proposed Model	***1.286***	***1.085***	***1.000***	***0.959***	***0.938***
	Flat Model	1.267	1.080	1.000	0.957	0.935
40	Davinci	1.193	1.064	1.000	0.976	0.958
	Proposed Model	***1.168***	***1.045***	***1.000***	***0.980***	***0.970***
	Flat Model	1.267	1.080	1.000	0.957	0.935
60	Davinci	1.156	1.051	1.000	0.981	0.968
	Proposed Model	***1.158***	***1.042***	***1.000***	***0.981***	***0.972***
	Flat Model	1.267	1.080	1.000	0.957	0.935
80	Davinci	1.145	1.046	1.000	0.983	0.971
	Proposed Model	***1.158***	***1.042***	***1.000***	***0.981***	***0.972***
	Flat Model	1.267	1.080	1.000	0.957	0.935

In this section, we describe the results of our comparison with TCAD simulations. The comparison structure is shown in Fig. 6. Table 2 shows results for various values of $\Delta L/2$ and Z', for W = 400nm, W' = 20nm. Table 3 shows the same results for W'=40nm. The accuracy is compared against a flat model where the threshold voltage is assumed to be the same across the entire device. The flat model is similar to that used in previous literature[1,2,3]. It is found that the variation in Ioff is considerable based on the location of the length variation and the flat model completely fails to predict this. The proposed model, on the other hand, is able to capture this dependency very well.

The data in the tables is shown in Fig 7 (a), (b), and (c) in graphical form as contour plots to indicate the dependence of Ioff on the location and the length of the irregularity. Plots for the model as well as the actual data are shown. Examining plots (a) and (b) reveals that the overhead trend is closely captured by our model. On the other hand, the flat model is completely unable to capture the large dependence on location, as shown by the contour plot of Fig 7(c).

Since the dependence of Ion on threshold voltage is very weak, we find no appreciable difference in Ion overheads for irregularities at different locations. Therefore, this model does not help particularly for Ion and we do not show results for the same.

6. CONCLUSIONS

To the best of our knowledge, this paper proposes the first location-dependent threshold voltage model to analyze irregular transistor gates due to imperfect lithographic patterns. These gates are found to have distinctly different Ioff and Ion characteristics compared to perfectly rectangular gates, and cannot be handled correctly by SPICE-like circuit analysis tools. We have recognized the fact that the threshold voltage is non-uniform across the device width and incorporated this effect into our model. It is found that the location of a particular irregularity along the channel significantly affects its impact on device characteristics. We have proposed a threshold voltage model that is simultaneously dependent on the location of a point along the channel as well as the length at that point. Using this

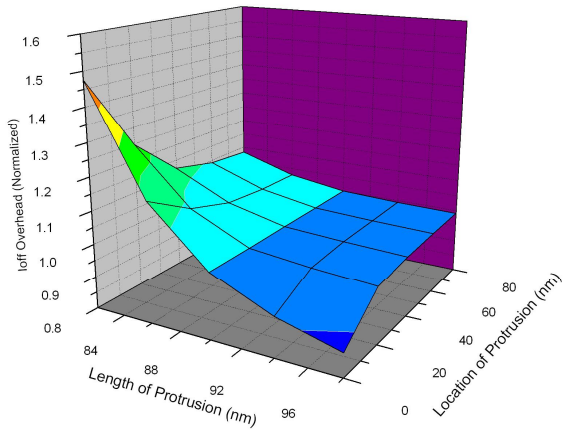

Fig 7a . Contour plot of observed data

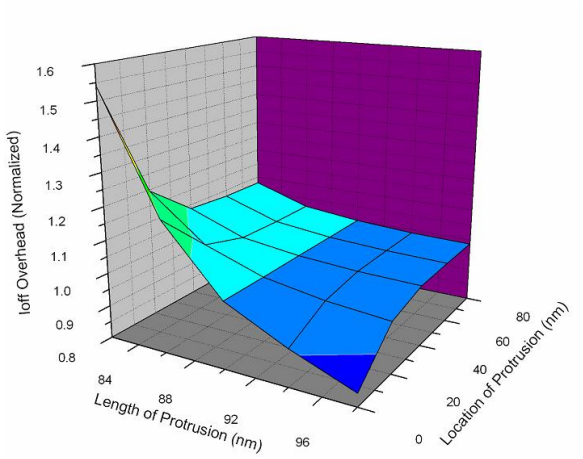

Fig 7b. Contour plot of fitted model

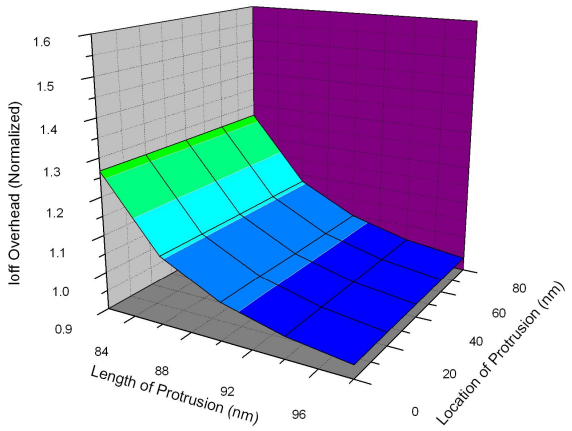

Fig 7c. Contour plot of flat model

model, we analyze non-rectilinear gates with various structures. Comparing our results with TCAD simulation results, we show that this method is considerably more accurate than a method that considers the threshold voltage to be flat along the channel. Future work in this area concentrates on improving the accuracy of this model and obtaining matching SPICE and TCAD setups for pure SPICE- based modeling.

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