Interaction and Balance of Mask Write Time and Design RET Strategies

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ABSTRACT

It has been demonstrated that the write time for 50keV E-beam masks is a function of layout complexity including figure count, vertex count and total line edge. This study is aimed to improve model fitting by utilizing all the variables generated from CATS. A better correlation of R^2 = 0.99 was achieved by including quadratic and interaction terms. The vertex model was then applied to estimate write time of various nano-imprint templates. Accuracy of the vertex model is much better than the numbers generated from E-beam tool software. A 90nm test layout was treated with a mask optimization (MO) algorithm. A 26% write time reduction was observed through shot count reduction. The advanced features of the new generation E-beam writing tool combined with mask layout optimization, allows the same level of mask cost even though the capital cost of the new tool set increased 25%.

Keyword: design for manufacturing, CATS, write time, OPC, data fracture, mask optimization

1. INTRODUCTION

Long write time is one of the main sources of rising mask costs. Our previous work [1] indicated that write time is a function of figure, vertex count and total line edge. This finding helps quantitatively predict write time before accepting a job and avoids unexpectedly long write times. In this work, more comprehensive model fitting was applied to improve accuracy (R^2). The vertex model was used to examine some real applications: write time of nano-imprint templates and the interaction between shot count reduction and write time.

A good write time estimator can be very useful in advanced technology development and planning. For example, it is very costly and time consuming to layout an actual device, run it through CATS and data fracture, and perform a write time estimation on a production e-beam writer. Our proposed model can be conducted completely offline from a production environment. The process flow runs as follows. First, a small design cell is generated. The cell is treated with MO. Shot counts of the cell with and without MO are obtained. The small cell is tiled to a full chip. CATS fragmentation is then performed on both files with and without MO, and vertex statistics are obtained. Write time can be drawn from a vertex model to include all the variables from the CATS calculation. For mask cost comparison, two process lines were used: a 90nm line with an early generation tool set and a 65nm line with state-of-the art equipment. Factors such as write time reduction through MO and variable speed stage from writing tools are employed in the cost analysis.

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2. WRITE TIME ESTIMATION

CATS fractures a layout into a machine write-ready format and generates statistical parameters. These variables, which are extracted from post-OPC layout data, include figure count, vertex count, vertex density, area, coverage and total line edge (TLE). Figure 1 is a pairwise scatter plot that shows the statistical relationship between actual write time (AWT) and different variables that quantify the complexity of a layout. A comprehensive write time estimator can be generated by including quadratic and interaction terms as shown in Figure 2. R^2 of 0.984 is achieved. It is now possible to predict write time of fractured data precisely without transferring the data to an e-beam writer and waiting for it's internal software to estimate write time.

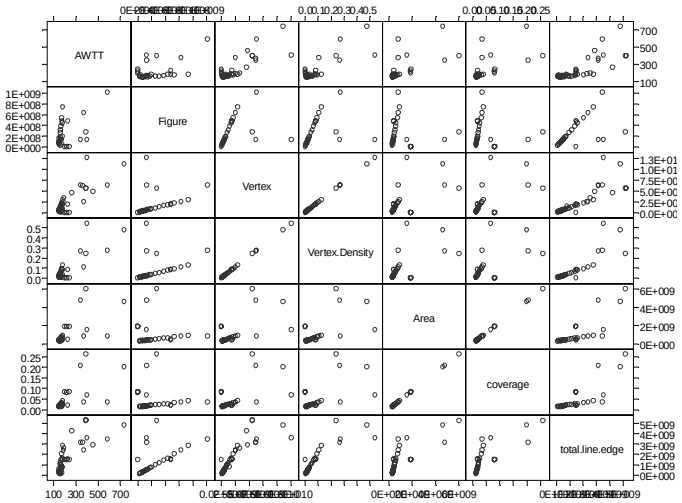

Figure 1. Pairwise scatter plot of actual write time and other layout variables.

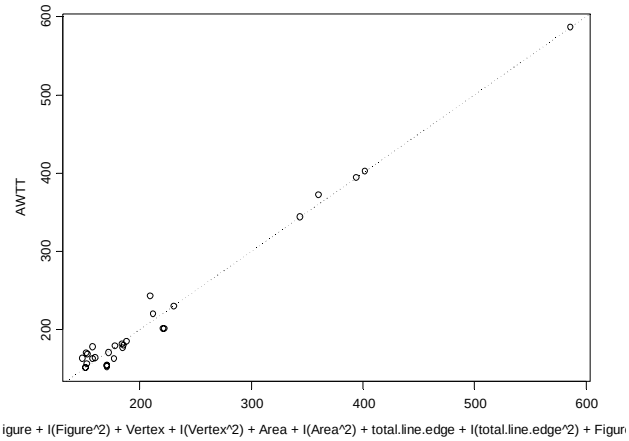

Figure 2. Write time as a function of figure, vertex, area and total line edge. R^2 of the fit is 0.984.

3. MODEL VALIDATION

In the first case study, we investigated the trade-off between various post designs versus write time for a nano-imprint lithography application. For imprint lithography, a circular-shaped post is preferred from a design point of view. However, from a mask making perspective, a square shape is recommended because it involves only a single shot per post. Initially, we experienced very long data fracture times and write times (Mask 1 in Fig. 3). Estimated write time from the e-beam writer software also had large discrepancies compared to the actual write time. On the other hand, our vertex-based model is very useful

in understanding the interaction between layout and write time. Vertex write time (VWT) based on the linear regression fit model matches actual write time (AWT) very well, as shown in Figure 3. Software from the e-beam writer consistently overestimated write time by more than 30%. The vertex model predicted write time precisely even though the total writing area and features changed from mask to mask.

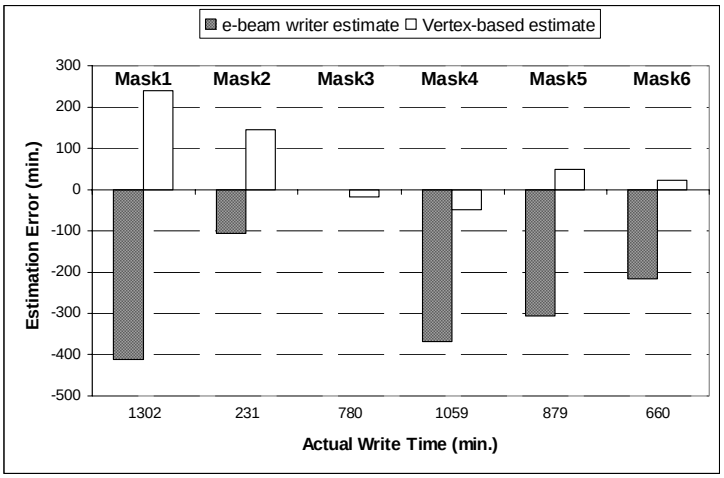

Figure 3. Comparison of actual write time versus e-beam writer estimate and vertex-based model estimate.

3. MASK OPTIMIZATION

In the second case study, a new algorithm called mask optimization [2] is applied to demonstrate design intent-driven reduction of RET complexity and estimated mask write time. A 90nm design rule was applied to illustrate the cost benefit with and without MO, based on estimated write times.

Each design cell has 180,158 instances that are equivalent to approximately 800,000 gates. The physical size is 1.3 X 1.3 mm on a wafer. The cell was tiled to a 20x10 array, representing a full chip with a reasonable field size on a wafer. There are two clocks in the design. Table 1 is the slack report showing pre and post optimization slacks. Metrics for non-optimized and optimized designs are listed in Table 2.

Table 1: Pre and post optimization slack.

Clock	Period	Slack (Non-optimized)	Slack (Optimized)
Clk1	10ns	+0.6042ns	+0.5952ns
Clk2	2ns	+0.2601ns	+0.1228ns

Table 2: Metrics for non-optimized and optimized designs.

Metric	Non-optimized	Optimized	Improvement
Shot Count	23491105	17424169	26%
OPC Runtime (seconds, wall time)	12353	7805	37%
File size (bytes, Gbit zipped)	168816506	136117133	19%

As can be seen, a significant reduction in shot count (26%) is achieved. Note that these reductions come from addressing gate poly only. No changes were made to field poly for this test. We expect that these results will improve when field poly optimization is included.

5. WRITE TIME ESTIMATION

The two data files were also run through CATS to collect vertex information. Several CATS formats including MODE5 flattened and hierarchy, VSB11 and MEBES were used to determine if there were any differences. VSB11 and MEBES formats are typically used in current mask production. It is found that

vertex count has a 28% reduction through mask optimization where other metrics such as figure count, area and TLE remain relatively unchanged. This result is consistent regardless CATS data format.

In addition, E-beam write manufacturers have made improvements in terms of write time reduction. Compared to previous generation E-beam tools (noted as Gen I), the new generation EB tools (Gen II Regular Mode) have much larger memory banks to handle large file sizes. Some tools also have the option of a variable speed stage (Gen II Fast Mode) where the mask stage can travel much faster if there is no pattern to write between two points. Figure 4 is a comparison of write times using different generations of writers with different mask stage speeds. On average, the variable stage speed mode runs about 20% faster than the regular mode. MO can save up to 32% on the write time on the same writing platform. An 8.5 hour job on a previous generation tool (tallest bar in Figure 4) without mask optimization requires less than 3 hours on the latest tool with fast mode and optimized layout (shortest bar in Figure 4)—a 60% write time reduction! Our initial development results show that there is no performance degradation in terms of CD and registration control from the regular mode to the fast mode. Layout optimization certainly gives mask makers another option for cycle time and cost reduction.

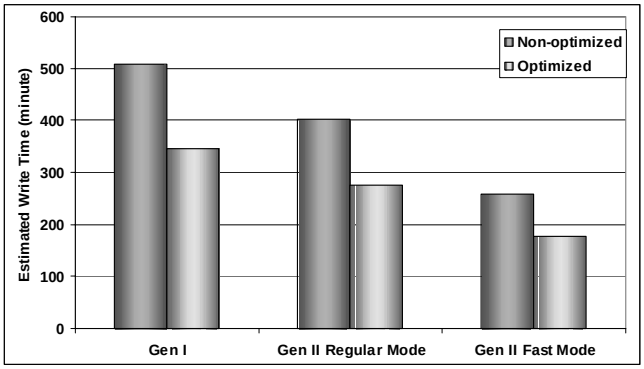

Figure 4. Write time comparison.

5.2 Mask Cost Analysis

For cost comparison, two process lines from current production were used: a 90nm line (Gen I) and a new 65nm line (Gen II). The 65nm line employs almost completely new equipment including an E-beam writer, etcher, bake and develop cluster, CD SEM, inspection tool, repair tool and cleaner. The capital cost of the new 65nm line is about 25% higher than the 90nm line. However, because of the write time reduction through mask optimization, it can offset the high capital cost if MO can be adopted. Figure 5 illustrates the idea. To minimize the impact of other variables, yield and profit margin are kept constant for both 90nm and 65nm lines. It can be seen that with MO, a mask can be written on the more advanced 65nm line with much better image fidelity, and maintain the same cost level as those written with previous generation tools. An 11% cost saving can be achieved from a mask written on a 90nm line without MO compared to a mask written on a 65nm line with MO.

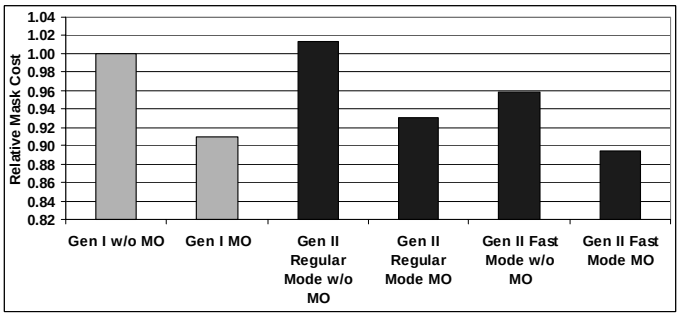

Figure 5. Mask cost comparison with or without mask optimization (MO).

Another potential benefit of MO is image fidelity improvement. This is hard to measure quantitatively or in terms of mask cost. Sliver control is important to retain pattern fidelity. Sliver reduction or optimized sliver placement can translate into better mask quality. When slivers can not be avoided, they should be placed inside the pattern rather than on the edges. Figure 6 illustrates the difference between placing a sliver in the middle of a pattern versus at the edge of the pattern. An edge sliver may cause CD errors or inspection problems.

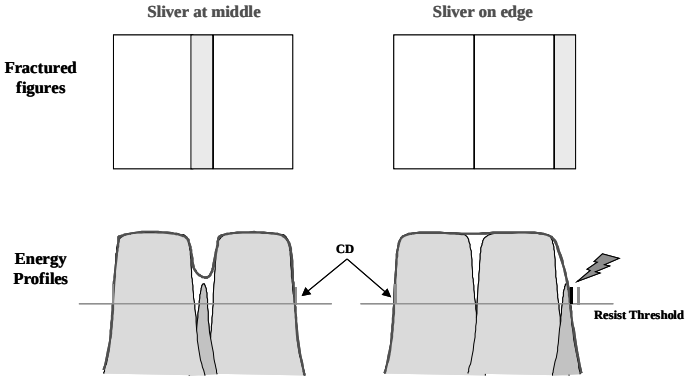

Figure 6. Comparison of sliver placement.

5. CONCLUSION

With all variables being considered, it is possible to improve the accuracy of a vertex-based write time estimation. The vertex model has demonstrated better accuracy than writer software through a real case application. With a mask optimization algorithm, shot count can be reduced by 26%. Write time can be reduced up to 60% if mask optimization and a fast writing mode can be employed. With MO, it is possible to produce a mask with a more advanced process line and still maintain the cost. This paper provides several options for masks with different tool sets, mask treatments and writing speeds.

6. ACKNOWLEDGEMENT

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7. REFERENCE

[1] Y. Zhang, R. Gray, S. Chou *et al*, "*Mask Cost Analysis via Write Time Estimation*", SPIE Microlithography Conference, 5756-31, San Jose, CA, Feb. 28 – March 4, 2005

[2] P. Gupta and A. B. Kahng, "*Improving OPC Quality Via Interactions Within the Design-to-Manufacturing Flow*", Photomask Japan, Yokohama, April 2005.