Wafer Topography-Aware Optical Proximity Correction for Better DOF Margin and CD Control

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ABSTRACT

Depth of focus is the major contributor to lithographic process margin. One of the major causes of focus variation is imperfect planarization of fabrication layers. Presently, OPC (Optical Proximity Correction) methods are oblivious to the predictable nature of focus variation arising from wafer topography. As a result, designers suffer from manufacturing yield loss, as well as loss of design quality through unnecessary guardbanding. In this work, we propose a novel flow and method to drive OPC with a topography map of the layout that is generated by CMP simulation. The wafer topography variations result in local defocus, which we explicitly model in our OPC insertion and verification flows. Our experimental validation uses 90nm foundry libraries and industry-strength OPC and scattering bar recipes. We find that the proposed topography-aware OPC can yield up to 90% reduction in edge placement errors at the cost of little increase in mask cost.

1. INTRODUCTION

As optical lithography advances into the 90nm technology node and beyond, minimum feature size outpaces the introduction of advanced lithography hardware solutions. In particular, the minimum depth of focus margin required for manufacturability of metal layers is extremely difficult to achieve due to nonplanar topography. A root problem is that predictable and systematic variation in depth of focus is not modeled or exploited during the application of advanced reticle enhancement techniques such as optical proximity correction (OPC) and subresolution assist feature (SRAF) insertion. From the designer standpoint, this results in unnecessary guardbanding, difficult performance closure, and wasted (area, delay, power) chip resources. To the extent that depth of focus is a determinant of "process window", several works in the literature dealing with process window-aware OPC are worth noting. A work of Cobb and Granik[15] proposes to solve for OPC at a nonzero defocus value to increase depth of focus (DOF), which is the amount of focus variation that can be tolerated while maintaining acceptable lithographic quality. The approach of[15] minimizes an objective that is a function of edge placement error (EPE) and image slope with respect to dose; EPE is the primary objective, and image slope is the secondary objective. The LithoCruiser OPC software from ASML MaskTools can optimize OPC solutions with critical dimension uniformity, median and yield as objectives. The approach entails Monte-Carlo simulation of focus and exposure with Gaussian distributions, and aerial image modeling to predict critical dimension. Unfortunately, these and other previous methods are oblivious to *systematic and predictable* focus variation that arises from layout-dependent wafer topography variation. Because deeply-subwavelength, high-NA (numerical aperture) lithography is very sensitive to defocus, wafer flatness has become a critical objective for fabrication processes. Chemical-mechanical planarization (CMP) is an enabling technique to achieve thickness uniformity of dielectric and conductor layers in the chip. Dummy fill insertion is a well-known technique to enhance the uniformity of layout feature density, so as to improve the planarization achieved by CMP.* Even after dummy fill insertion, there is a great deal of remaining post-CMP topographic variation which is manifested

*Dummy fill insertion changes the coupling and total capacitance of interconnects,[3] and thus itself induces design closure issues. However, in this work we do not address the question of improved fill synthesis to reduce topographic variation.

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as dielectric erosion and metal dishing. Post-CMP thickness variations are known to have a severe impact on the stability of downstream process steps, and ultimately on yield.[4] Defocus corresponding to this thickness variation severely affects patterning of the subsequent upper layer.[†]

Optical proximity correction (OPC) is a widely used resolution enhancement technique for control of critical dimension (CD). With OPC, photomask shapes are deliberately distorted to compensate for differing amounts of pattern information diffracted at various pitches. Beyond the 130nm node, subresolution assist feature (SRAF) based OPC with off-axis illumination (OAI) achieves improved DOF margin. However, tightly prescribed spacing - in particular, assist-to-main pattern and assist-to-assist - are needed to prevent SRAFs from printing.[10] Such layout design constraints result in forbidden pitches with significantly lower printability in certain DOF values.[7] Thus, the industry faces ever-deeper interactions between planarization, defocus, and correct deployment of OPC. Our present work is motivated by the fact that current OPC techniques do not consider topography, and that this incurs a very large process variability cost. We describe a novel methodology for *topography-aware OPC* (TOPC) to directly control the CD error that is induced by a nonplanar topography. Different defocus values in a chip are predicted by thickness values which are extracted by CMP simulation. Then, all metal lines with different defocus values are corrected by OPC with different optical/resist models. As a result of the TOPC methodology, we observe significant reduction in CD error, as evaluated by industry-strength OPC and verification flows at the 90nm node. In this paper, we first present various analyses of lithographic printability for nonplanar topography. We then propose a general methodology for TOPC. Our main contributions are as follows.

- We introduce a novel OPC technique that is aware of post-CMP wafer topography variation. This technique achieves substantial improvement in DOF margin and CD control.
- The TOPC method may lead to poor correction of patterns that are located on the boundary of different DOF values, because one pattern is affected by the other (at an incorrect assumed defocus) during the OPC insertion. We assign DOF values to layout features using a reduction to maximum-flow, so as to prevent closely spaced patterns from being assigned different defocus values, while yet maintaining fidelity to the topography map.

2. DETAILED MOTIVATIONS FOR TOPC

We motivate our work on TOPC with Figure 1(a), which shows how dense regions (e.g., in copper-oxide polishing) will have *predictably* larger post-CMP thickness compared to sparse regions. The depth-of focus (DOF) variation corresponding to the thickness variation severely affects metal patterning of the subsequent upper layer, as shown in Figure 1(b) (results obtained using SOLID-C lithography simulation from Sigma-C).

2.1. Standard vs. Topography-Aware OPC and ORC

We also motivate wafer topography-aware OPC by considering the disconnect between focus-awareness and focus-unawareness, not only in the OPC insertion but also in the optical rules checking (ORC) step that checks post-OPC printed images against drawn shapes. We distinguish two kinds of OPC methodology, *standard* and *topography-aware*. In standard OPC (SOPC), the assumption is that any particular layer is flat and therefore a defocus value of zero is considered for that layer. This incorrect assumption will lead to CD variation of the metal feature that will be placed on that layer. To clearly illustrate the CD variation in SOPC, Figure 2 compares the resist image of metal lines in $0.0\mu m$ DOF with the image in $-0.3\mu m$ DOF. CDs of metal lines in $-0.3\mu m$ topography cannot be corrected by the SOPC with zero defocus even if the CD degradation after the OPC is somehow better than that before OPC. On the other hand, if the thickness variation of the layer is taken into account, OPC can adjust its process accordingly. Considering OPC and ORC together, there are four combinations, shown in Table 1. We explore the effectiveness of each combination separately in the following discussion.

[†]There is dielectric deposition and resist spin-on after CMP, and the profile following these two steps is a more accurate representation of the wafer's defocus map. In the present work, we assume that the deposition and spin-on processes conform to the post-CMP profile, as is typically the case.

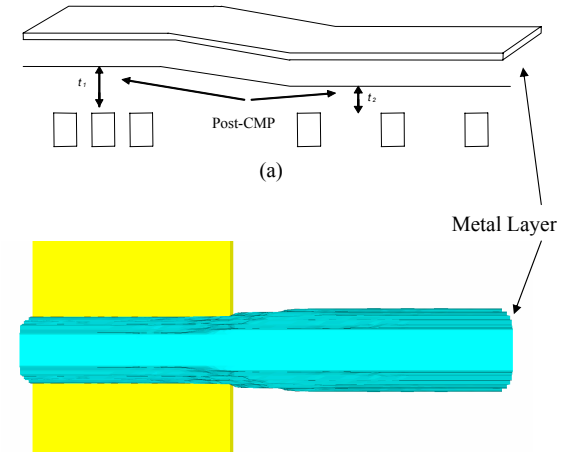

Figure 1. (a) Side view showing thickness variation over regions with dense and sparse layout. (b) Top view showing CD variation when a line is patterned over a region with uneven wafer topography, i.e., under conditions of varying defocus.

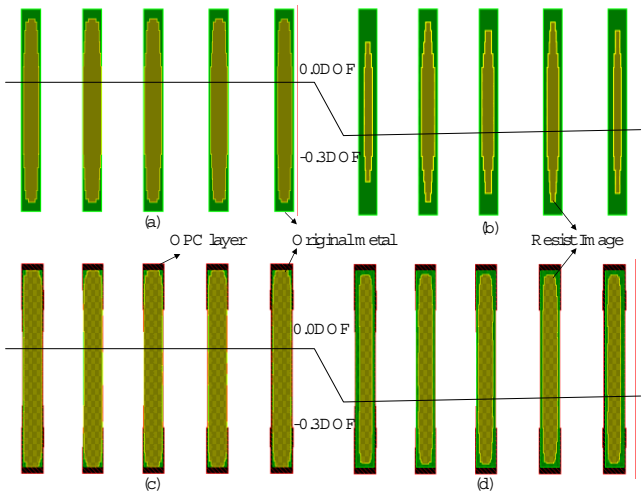

Figure 2. Standard OPC simulation: (a) original layout and simulation result with zero DOF model, (b) original layout and simulation result with -0.3μm DOF model in the nonplanar topography, (c) standard OPC layout and simulation result with zero defocus model, and (d) standard OPC layout and simulation result with -0.3μm DOF model in the nonplanar topography.

OPC method	ORC method	Δ CD (Drawn vs. Printed)
STD	STD	~ 0
STD	T-A	> 0
T-A	STD	> 0
T-A	T-A	~ 0

Table 1. Four different combinations of OPC and ORC: STD and T-A respectively indicate standard and topography-aware methodologies.

In Table 1, STD and T-A stand for standard and topography-aware methodologies, respectively. To explain these combinations, assume that in 90nm technology, the maximum allowable defocus value is +/-0.3um (ΔD)

for manufacturing. We also refer to the thickness variation of the layer as X. We wish to make the case that when topography-aware OPC and ORC are employed, CD variation will be minimized.

- Figure 3(a) shows the case when the combination of standard OPC and standard ORC is used. Standard OPC ignores thickness variation, hence a defocus value of 0 is assigned to the layer $T0$. If there is no thickness variation, this combination leads to a small CD variation because OPC can easily exploit the pitch dependency of CD. However, the problem with this method is that the premise of an even topography is wrong. In other words, due to CMP process effects, the layer is not exactly flat.
- Figure 3(b) shows the case when SOPC is used with topography-aware ORC (TORC). In this case, there is still no consideration of thickness variation during the OPC process, but ORC is aware of the topography, which changes the maximum allowable defocus value set by ORC. In general, the maximum allowable defocus value set by topography-aware ORC is derived as (T_i +/- ΔD) where T_i is the defocus value set for each specific region of the layer and ΔD is the maximum allowable defocus value set by standard ORC. Since SOPC assigns zero defocus to the layer, the maximum allowable range for ORC is just +/- ΔD. On the other hand, TORC has been adjusted according to the topography. In Figure 3b, we assume that T_0 has zero defocus and T_1 has -0.1μm defocus. This changes the maximum allowable defocus value set by ORC; for T_0 we have a range of -0.3 to 0.3 and for T_1 the range is from -0.4 to 0.2. Since the allowable range for SOPC is from -0.3 to 0.3, we will have CD variation generated at T_1 due to mismatch between the OPC and ORC.
- The third combination, which employs TOPC and standard ORC, is not of interest: as with the first combination, the entire premise of the method is faulty. Since OPC is aware of the topography, it will adjust accordingly, but standard ORC will not consider the changes. For example, T_1 that has a defocus value of -0.1 will have an allowable defocus range of -0.4 to 0.2, but standard ORC still considers a range of -0.3 to 0.3. This will again lead to CD variation of the metal feature.
- The final combination should yield the best result, because both the OPC and ORC are aware of the topography and therefore can adjust accordingly. For example, T_0 will have an allowable defocus range of -0.3 to 0.3 whereas T_1 will have a defocus range of -0.4 to 0.2. Thus, the pattern on T_1 will meet CD tolerance with -0.4μm DOF.

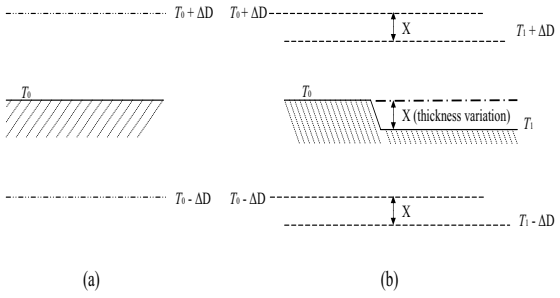

Figure 3: Combinations of standard and topography-aware OPC and ORC.

2.2. Cost and Quality of OPC

Increased application of OPC makes mask data preparation (MDP) difficult: figure counts explode as dimensions shrink and RETs are more heavily used.[8] To optimize the data volume, conventional OPC hierarchically reorganizes the input GDSII data by reducing the redundant representation of identical cells.[11] The spatial context consisting of such identical cells is a unit as the proximity correction process evaluates effects due to adjacent or nearby features within the optical radius of influence. Thus, identical contexts are corrected only once, which helps reduce correction time and data volume. Our proposed TOPC methodology affects

hierarchical decomposition of the layout because "context" must now be with respect to both the proximity effect of neighboring patterns, and the DOF values of the topography. In particular, identical patterns that are assigned to different DOF values no longer exist within the same context, and all context information should be newly constructed according to patterns that have the same DOF value. In the TOPC methodology, all figures are partitioned among a relatively small number of DOF values. The number of DOF values used in this partitioning (see the discussion of "defocus marking layers", below) must be carefully considered, as increasing this number negatively impacts data volume and OPC runtime, even as TOPC achieves better CD control and DOF margin.

3. TOPC METHODOLOGY

Our new TOPC methodology informs OPC insertion by estimated defocus values derived from simulation of the *chemical-mechanical planarization* (CMP) process. After fabrication of a given chip layer, variation in topography creates focus variation in the lithography used to create the next layer of the chip. We use CMP simulation to compute a topographic map over the chip layout; this yields for each layout feature an associated height $h(f_i)$. Commercial CMP simulation software is available from companies such as Praesagus.[13] In our current implementation, we use a CMP simulation model derived from the Ph.D. thesis of Tugbawa.[14] The overall TOPC methodology, as distinguished from standard OPC (SOPC), is summarized in Figure 4.

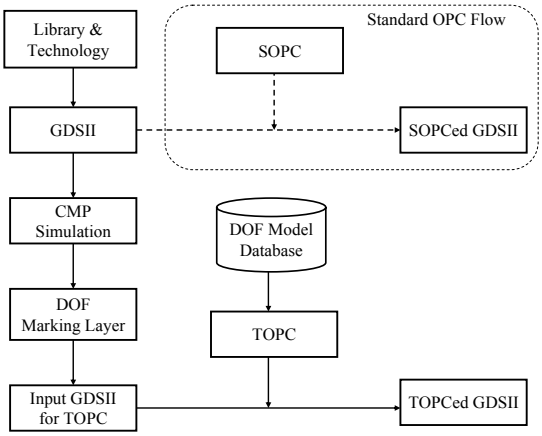

Figure 4. The modified design and evaluation flow: a map of thickness variation from CMP simulation is converted to defocus marking layers and then fed into GDSII for TOPC.

3.1. Defocus Marking Layer (DML) Assignment

While the CMP simulation yields a continuous topographic map, it is necessary to use only a small number of discrete defocus values when calculating the OPC solution. Thus, the central problem is to assign one of the available defocus values to each layout feature, while reflecting the topographic map as accurately as possible. In our methodology, every layout feature f_i is associated with a *defocus marking layer*, $DML(f_i)$, which indicates the defocus value (e.g., +0.1 μm) which is assumed during the calculation of reticle enhancement (e.g., optical proximity correction or phase-shifter shapes) for f_i. However, applying two different OPC models to two adjacent patterns on some boundary will increase CD variation compared to using an "average" DOF model. For example, to correct one pattern on the $0.1\mu m$ DML boundary, the pattern should refer to the image of other patterns on the $0.2\mu m$ DML boundary. However, these other patterns are being simulated by a $0.1\mu m$ DOF model instead of a $0.2\mu m$ DOF model. In this case, CDs of the two patterns can be more distorted than it, e.g., we apply to all patterns a $0.15\mu m$ DOF model that is the average of the two models. Accuracy of reticle enhancement (as well as inherent limitations of OPC software) requires that $DML(f_i) = DML(f_j)$ for all features f_i, f_j whose inter-feature distance $d(f_i, f_j) \leq R$, where R is the "optical radius" of the lithography

Input: Layout data in GDSII Stream format, optical radius R,
defocus marking layer thresholds $Th_1 < Th_2 < ... < Th_{2k-2}$

Output: Partition of all features into k DMLs

1. Use CMP simulation to compute the post-CMP topography
2. From the topography, determine the height $h(f_i)$ for each feature f_i
3. Construct a flow network topology $N = (V, E)$ with a vertex v_i for each feature f_i, a super-source S and a super-sink T, and an edge $e_{i,j}$ between two vertices v_i and v_j if $dist(f_i, f_j) < R$
4. **For** $(i = 1; i < k; i{+}{+})$
5. Calculate edge capacities in the flow network N as follows
   (A) If $h(f_i) \leq Th_{2i-1}$, there is an infinite-capacity edge from S to v_i.
   (B) If $h(f_i) \geq Th_{2i}$ then there is an infinite-capacity edge from v_i to T
   (C) If $Th_{2i-1} < h(f_i) < (Th_{2i} + Th_{2i-1})/2$, then there is an edge from S to v_i with weight w
   (D) If $(Th_{2i} + Th_{2i-1})/2 \leq h(f_i) < Th_{2i}$, then there is an edge from v_i to T with weight w
   (E) For all edges $\in N$, edge capacities are given by the weights $w(e_{i,j}) = \lfloor \frac{R}{dist(f_i, f_j)} \rfloor$
6. Calculate a maximum S-T flow in the edge-capacitated flow network N.
   The maximum flow saturates a min-weight cut
7. All vertices on the S side of the cut are assigned to DML i and deleted from N
8. The remaining vertices are assigned to DML k

Figure 5: k-DML Assignment Methodology

process.[‡] The inter-feature distance requirement of the DML assignment can be captured using a graph in which each feature is represented by a vertex, and there is an edge between two vertices if the distance between their corresponding features is less than R. We may further assign weights to edges in this graph, with higher edge weights corresponding to pairs of features that are closer to each other. The other requirement is that every feature should be assigned to the DML partition to which it belongs if possible.

We formalize the problem of assigning features to k DMLs as follows. Given a set of vertices $V = \{v_1, v_2, \ldots, v_n\}$ with height function $h : V \rightarrow Z^+$, a set of weighted edges $E \subseteq V \times V$, and $2k-2$ threshold values $Th_1, Th_2, \ldots Th_{2k-2}$. The minimum value of $h(v)$ is Th_0 and the maximum value of $h(v)$ is Th_{2k-1}. All feature vertices with $Th_{2i-2} \leq h(v) \leq Th_{2i-1}$ $(i = 1, ..., k)$ are assigned to Partition i (DML i). Each remaining vertex for which $Th_{2i-1} < h(v) < Th_{2i}$ $(i = 1, ..., k-1)$ is assigned to either Partition i or Partition $i+1$, such that the total edge weight crossing the cutline is minimized. Finally, we can determine an *optimal* assignment of features to k DMLs via $k-1$ *minimum cut* calculations in a network. Our methodology for assignment of features to k DMLs is detailed in Figure 5.

3.2. TOPC Validation and Limitations

To complement the discussion of Section 2.1, we now present our methodology to validate the quality of result (QOR) of TOPC using commercially available ORC software. We also discuss some practical limits of TOPC as deployed using current commercial software tools. Suppose OPC enables all patterns to satisfy a given CD tolerance for manufacturing, generally +/- 10% of each pattern size, at some given worst-case defocus. Then, the maximum allowable defocus range, ΔD, and the threshold are determined according to the region where there are zero CD violations with ORC. We compare QOR of TOPC and standard OPC as follows.

- We calculate different worst defocus values based on DOF marking layers, i.e., the value is the sum of the DOF value of the marking layer and ΔD.
- We apply the different values to all patterns according to the DOF marking layer assignment.

[‡]This requirement grows stronger as the inter-feature distance $d(f_i, f_j)$ decreases. In modern lithography processes, typical values of R are on the order of one micron or less.

- We compare the number of CD violations arising with standard OPC and TOPC, respectively.

To validate the TOPC methodology we look at only two combinations: (1) STD OPC / T-A ORC, and (2) T-A OPC / T-A ORC. We do not consider the other two combinations, because (as discussed in Section 2.1) they are based on incorrect premises.[§] Since current commercially available OPC software tools do not consider topography, we are not able to apply the TOPC methodology to features that lie on the boundary between two different defocus values. Figure 6 shows the regions to which TOPC will be applied, as well as the regions to which it cannot be applied due to commercial OPC tool limitations. In this figure, the hatched areas are those to which TOPC will be applied; these are designated with X and Y defocus values. The distance between each of the regions to which TOPC will be applied is equal to the optical diameter. Despite this constraint, we show in the next section that TOPC substantially reduces CD error in regions where it can be applied. Furthermore, our DML assignment algorithm effectively limits the number of features to which TOPC cannot be applied.

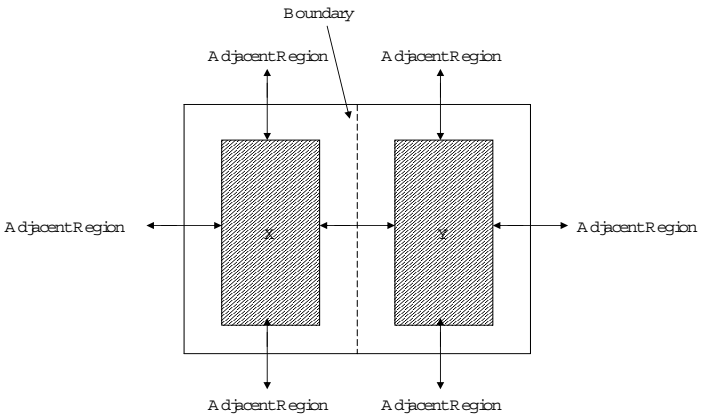

Figure 6: TOPC validation regions.

4. EXPERIMENTS AND RESULTS

We use two benchmark designs in our experiments. The first benchmark (Benchmark1) is the $alu128$ core with $1.1K$ instances from *Opencores* in *Artisan TSMC 0.09µm* libraries using *Synopsys Design Compiler v2003.06-SP1*. The synthesized netlists are placed with row utilization of 90% using *Cadence First Encounter v3.3*. The second benchmark (Benchmark2) consists of *aes* and *des* cores with 189K instances and 65% utilizatoin in the *Artisan UMC 0.09µm* library. All designs are trial routed before running timing analysis. On the lithography side, we use *Sigma-C SOLID-C* to check CD. *Mentor Graphics Calibre* is used for model-based OPC, SRAF OPC and optical rule checking (ORC). TOPC is performed based on the DMLs. First, we apply the method to typical design of metal layer to verify enhancement of DOF margin and CD control. Figure 7 shows the simulation results of a metal shape with $0.14\mu m$ linewidth and $0.9\mu m$ space. There are four different curves from 0 to 0.4 which represent OPC patterns applied to 5 different DOF models. CDs of five different OPC patterns are plotted with the results of lithography simulation using $0.0\mu m$ to $0.6\mu m$ DOF models. In the SOPC method, if the pattern is located at $0.3\mu m$ topography and corrected with $0.0\mu m$ OPC model, the pattern will violate CD tolerance, which is typically +/-10% of CD. In other words, if a pattern has topographic variation outside of +/- $0.3\mu m$, or total DOF error (including wafer stage error) exceeds $0.3\mu m$, then the pattern fails tolerance criteria and will contribute to yield degradation. On the other hand, if we apply TOPC with $0.3\mu m$ DOF model to the pattern, the DOF margin within the CD tolerance obtains an additional $0.1\mu m$ DOF.

[§]With STD OPC / STD ORC, the assumption is that there is no thickness variation, which is obviously unrealistic. With T-A OPC / STD ORC, the OPC tool is aware of the topography, but the ORC is still based on the assumption that every point of the layer has zero defocus value. This will fail to match with the allowable defocus range used by T-A OPC.

Table 2 summarizes the experimental results. In this table, DOF range is the maximum DOF range of the pattern in a particular topography, which can be measured according to + and - directional DOF variation. For example, if a pattern is located at $0.2\mu m$ topography, + directional DOF ranges of the pattern are $0.05\mu m$ with SOPC and $0.12\mu m$ with TOPC. Thus, the pattern increases + the directional DOF range by $0.07\mu m$ after TOPC with $0.2\mu m$ DOF model, and the total DOF range of TOPC increases by $0.14\mu m$ compared to that of SOPC.

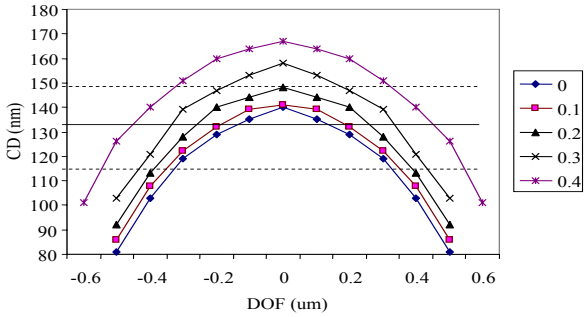

Figure 7: Comparison of DOF and EPE improvements with $0.14\mu m$ linewith and $0.9\mu m$ space.

OPC method	Topography (thickness: μm)	- directional DOF range	+ directional DOF range	Total DOF range
SOPC	0.0	0.25	0.25	0.50
SOPC	0.1	0.35	0.15	0.50
SOPC	0.2	0.45	0.05	0.50
SOPC	0.3	0.48	0.00	0.48
TOPC	0.0	0.25	0.25	0.50
TOPC	0.1	0.38	0.18	0.56
TOPC	0.2	0.52	0.12	0.64
TOPC	0.3	0.49	0.09	0.58

Table 2: Comparison of DOF margin with TOPC and SOPC.

For the Benchmark1 testcase with 6127 features, we implemented the k-DML assignment methodology (Figure 5) with $k = 3$ using C++. The optical radius R is $0.64\mu m$. The threshold values are 0.0998, 0.1002, 0.1998, and $0.2002\mu m$. All tests are run on a hyper-threaded Intel Xeon 2.4GHz CPU. The calculated maximum thickness variation of Metal 2 is 0.26 μm and the runtime is 0.36s. Based on maximum thickness variation of $0.26\mu m$, we can generate three different DMLs with $0.1\mu m$ step size for Metal 3. DML 0 represents all metal lines with topography thickness of $0.0\mu m$ to $0.1\mu m$. DML 1 has metal lines with added $0.1\mu m$ thickness variation, i.e., $0.1\mu m$ to $0.2\mu m$. DML 2 is similarly assigned. We also test our proposed algorithm using the Benchmark2 testcase with 933985 features. Since the calculated maximum thickness variation of Metal 2 is $0.36\mu m$, we assign four different DMLs with $0.09\mu m$ step size to all the features of Metal 3. The threshold values are chosen as 0.0898, 0.0902, 0.1798, 0.1802, 0.2698 and 0.2702 μm. The total DML assignment runtime is 38.7s. We assume maximum DOF variation to be composed of topography variation (50% contribution) and other factors (50%). In the Benchmark1 testcase, topography contribution, half of total thickness variation, is $0.13\mu m$. We construct two testcases based on the Benchmark1 library, which are shown in Figure 8.

- *CASE I.* Assume the stepper machine focuses on the average of the topography; This is DML1 in our case.
- *CASE II.* Assume the stepper machine focuses on DML2. Therefore, DML0 corresponds to -0.2μm defocus.

Assuming that the Bossung plots are symmetrical about $0\mu m$ defocus, (i.e., -0.13μm and $0.13\mu m$ are considered the same as shown in Figure 8), metal lines have two different DOF values in CASE I and three different values in CASE II. During TORC, the non-topography factors (ΔD) account for 0.13 μm defocus. As a result,

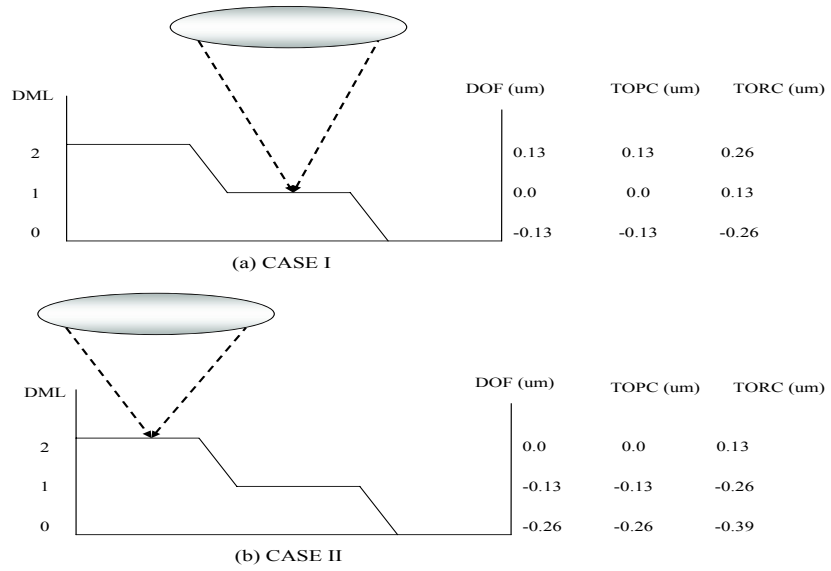

Figure 8: The Benchmark1 testcases.

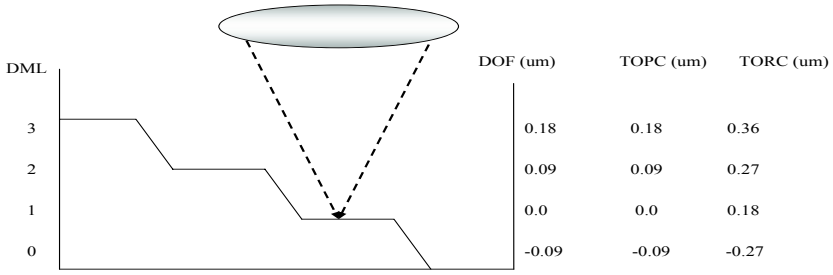

Figure 9: The Benchmark2 testcase.

a feature with $0.1\mu m$ thickness value (stepper focusing on $0\mu m$) in TORC will have worst-case DOF range of -$0.26\mu m$. Each OPC'ed metal line is evaluated by TORC with DOF models, i.e., $0.13\mu m$, $0.26\mu m$, and $0.39\mu m$. We apply the same methodology to the Benchmark2 testcase. The testcase has three different DOF values as shown in Figure 9. Topography and non-topography factors (ΔD) contribute to 0.18 μm defocus. Therefore, the worst case DOF range with the topography having $0\mu m$ defocus is 0.18 μm, and the OPC'ed metal line is evaluated by TORC with DOF models $0.18\mu m$, $0.27\mu m$, and $0.36\mu m$.

Table 3 shows the results of SOPC and TOPC according to EPE count, which is the number of edge fragments on metal having greater than 10% CD error. TOPC can reduce EPE count by between 68% and 80% versus the standard OPC flow. The improvement in process window and potential yield comes at the cost of some increase in data volume and OPC runtime, which is shown in Table 4.

Testcase		SOPC	TOPC	Improvement(%)
Benchmark1	CASE I	4652	1510	67.5
Benchmark1	CASE II	12855	3295	74.3
Benchmark2		52029	10198	80.4

Table 3: Comparison of EPE counts width SOPC and TOPC

Testcase		Original GDS (MB)	SOPC GDS (MB)	SOPC Runtime (min.)	TOPC GDS(MB)	TOPC Runtime (min.)
Benchmark1	CASE I	5.0	7.2	17	9.2	21
Benchmark1	CASE II	5.0	7.2	17	9.4	22
Benchmark2		696.2	2706.7	3351.1	3073.4	3459.7

Table 4. Comparison of OPC runtime and data volume between SOPC and TOPC. Note that SOPC result does not change between CASE I and CASE II.

5. CONCLUSIONS AND ONGOING WORK

In this work, we have proposed the first methodology for wafer-topography aware OPC. With an experimental testbed of 90nm foundry libraries, industry OPC recipes, and commercial OPC and ORC software tools, we have confirmed that our technique achieves up to 80% reduction in edge placement errors at worst-case defocus. With dimensions scaling faster than the lithographic process, depth of focus and hence awareness of topographic variation in RET will become increasingly important. Thus, we believe that topography-aware techniques such as ours will be critical for reducing parametric variation - particularly of interconnect performance - in future technology nodes. Our ongoing work is in the following directions.

- As TOPC will significantly reduce CD uncertainty, there will be a corresponding reduction in uncertainty of RC parasitics. Our current research investigates the impact of such a CD error reduction on RC parasitics of the circuit. We are also exploring new interconnect design methodologies based on the concept and results of TOPC.
- Lithographic process window is one of the most important reasons for stringent requirements for the CMP and dummy fill processes. A topography aware OPC flow will enable reduction in layout density control requirements, and hence the design impact (e.g., capacitive coupling overhead) of dummy fills. We are investigating the interaction between dummy fill and OPC in this context.
- Assist features are inserted in the OPC flow to increase depth of focus of isolated features. TOPC uses more accurate "nominal" focus values locally, and this can lead to a reduction in the complexity of assist feature insertion flows. We are currently investigating this synergy.
- We are currently investigating ways in which the DML partitioning flow can be made more design-aware. For example, there are several ways in which timing and power constraints can inform the steps of DML construction and feature assignment to DMLs.
- Finally, we are investigating improved TOPC and TORC flows to handle geometries at the edges of a DML (recall that we currently ignore such geometries).

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