Detailed Placement for Improved Depth of Focus and CD Control

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Abstract— Sub-resolution assist features (SRAFs) provide an absolutely essential technique for critical dimension (CD) control and process window enhancement in subwavelength lithography. However, as focus levels change during manufacturing, CDs at a given "legal" pitch can fail to achieve manufacturing tolerances required for adequate yield. Furthermore, adoption of off-axis illumination (OAI) and SRAF techniques to enhance resolution at minimum pitch worsens printability of patterns at other pitches. This paper describes a novel dynamic programming-based technique for *Assist-Feature Correctness* (AFCorr) in *detailed placement* of standard-cell designs. For benchmark designs in 130nm and 90nm technologies, AFCorr achieves improved depth of focus and substantial improvement in CD control with negligible timing, area, or CPU overhead. The advantages of AFCorr are expected to increase in future technology nodes.

I. Introduction

Optical lithography has been a key enabler of the aggressive IC technology scaling implicit in Moore's Law. Minimum feature sizes have outpaced the introduction of advanced lithography hardware solutions, so that gate length and CD tolerances prescribed in the 2003 International Technology Roadmap for Semiconductors (ITRS) [1] are extremely difficult to achieve. As a result, resolution enhancement techniques (RETs) such as optical proximity correction (OPC), phase shift masks (PSM), and OAI are being pushed ever closer to fundamental resolution limits [2]. Combinations of these techniques can provide certain advantages for lithography manufacturing, e.g., OAI and OPC, together with SRAF, achieve enhanced CD control and focus margin at minimum pitch.

However, when OAI is used, there will always be other (non-minimum) pitches for which the angle of illumination works with the angle of diffraction to produce a bad distribution of diffraction orders in the lens. These pitches are called *forbidden pitches* because of their lower printability, and designers should avoid such pitches in the layout. However, it is very difficult to consider all possible forbidden pitches in the design stage, particularly since the forbidden pitches are dependent on optical conditions which are often tuned in manufacturing. The resulting *forbidden pitch problem* for the manufacturing-critical poly layer must be solved before detailed routing, since routing "locks in" the poly layer layout. At the same time, we wish to address the forbidden pitch problem as late as possible, to avoid extra rework upon modification of the manufacturing process recipe. In this paper, we describe a novel dynamic programming-based algorithm for *AFCorr* (Assist-Feature Correctness), which uses flexibility in detailed placement to avoid forbidden pitches and the manufacturing uncertainty that they cause.

A. Related Works

We now review previous works related to forbidden pitches and their design implications. Socha et al. [3] observe that under more aggressive illumination schemes such as annular and quasar illumination, some optical phenomena become more prominent, most notably the forbidden pitch phenomenon. Shi et al. [4] give a theoretical analysis of pattern distortion in forbidden pitches, due to destructive light field interference. Although SRAFs are an effective method to collect high-order diffraction on the entrance pupil plane of a projection lens [5], Shi et al. report that incorrect SRAF placements around a given main feature can actually degrade the process latitude of that feature. A number of previous works have proposed techniques to control forbidden pitches using optimization of optical conditions such as numerical aperture (NA) and illuminator aperture shape of OAI [6, 7].

B. Contributions of This Work

In this paper, we first present various analyses of lithography printability within the context of the standard cell based design methodology. Our goal is to minimize CD variation error and enhance feature printability and reliability. Our main contributions are as follows.

- The adoption of model-based OPC implies that the post-OPC correction bias may lead to unintended printing of assist features. Thus, SRAF rules should be adjusted for typical post-OPC linewidths and spaces. In this context, we give a more realis-

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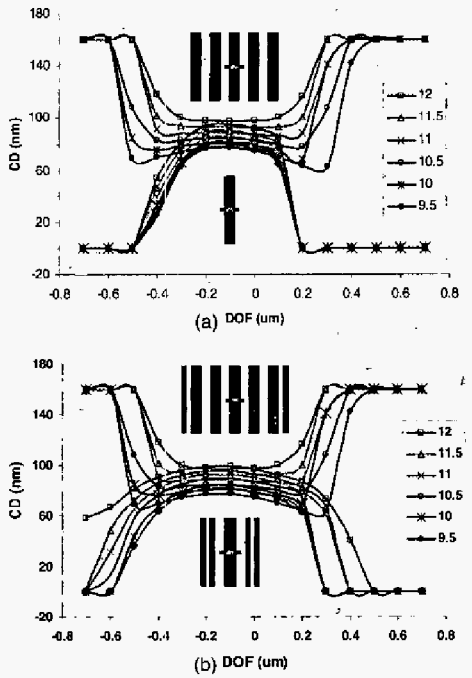

Fig. 1. Comparison of Bossung plots between dense and isolated lines : (a) results of Bias OPC and (b) results of SRAF OPC.

tic methodology for forbidden pitch extraction and SRAF insertion rule generation.

- We propose a novel post-detailed placement perturbation algorithm for *Assist-Feature Correctness* (AFCorr). AFCorr uses efficient dynamic programming methods to remove forbidden pitches in a given detailed placement. In conjunction with intelligent process-aware library layout, this technique can achieve substantial improvements in depth of focus (DOF) margin and CD control.

C. Organization of the Paper

The remainder of this paper is organized as follows. In Section 2, we review RET and its layout impact, focusing our discussion on strong OAI and OPC with SRAF. Section 3 introduces the proposed post-placement perturbation technique. Evaluation flows to validate its impact on lithographic manufacturability and experimental results are described in Section 4. We conclude in Section 5 with directions for ongoing research.

II. RET and Layout Impact

The extension of optical lithography beyond the quarter-micron regime has been enabled by a number of reticle enhancement techniques. These RETs address the available three degrees of freedoms in lithography, namely: aperture, phase, and/or pattern uniformity [10]. However the adoption of different RETs dictates certain tradeoffs with various aspects of process and performance.

Off-axis illumination (OAI) brings light to the mask at an oblique angle. As the angle of diffraction through certain aperture shapes matches a given pitch, higher-order pattern information can be projected on the pupil plane as determined by the numerical aperture (NA) of the illumination system. This technique enables the smallest pitch on the mask to obtain higher resolution and extended focus margin. However, other pitches beyond the optimum angle will have a *lower* process margin compared to conventional illumination (i.e., with a circular aperture). Since strong OAI is an essential technique in current lithography, these pitches should be forbidden; their avoidance is a new challenge for physical design automation. OPC is the deliberate and proactive distortion of photomask shapes to compensate for systematic and stable patterning inaccuracies. *Bias OPC*, the most common and straight-forward application of OPC, has proved to be a useful technique for matching photoresist edges to layout edges with essentially a layout sizing technique. However, bias OPC has limitations in enhancing process margins with respect to depth of focus and exposure dose. The Bossung plot[1] in Figure 1 shows that bias OPC is not sufficient to reduce the CD difference between isolated and dense patterns with varying focus and exposure dose. The CD distortion in the isolated pattern is usually a problem since lithography and RET recipes are not tuned or optimized for isolated lines [11]. The *SRAF OPC* technique combines pattern biasing with assist feature insertion to compensate for the deficiencies of bias OPC. SRAFs (or, Scattering Bars (SB)), which are extremely narrow lines that do not actually print on the wafer, modify the wavefront and allow the lens pupil to receive higher-order pattern information. The SRAFs are placed adjacent to primary patterns, such that a relatively isolated primary line behaves more like a dense line. This works well for bringing the lithographic performance of isolated and dense lines into agreement. The DOF margin of the isolated line as shown in Figure 1(b) is considerably improved from that shown in Figure 1(a), and a larger overlap of process window[2] between dense and isolated lines is achieved.

The key observation is that the SRAF technique places more constraints on the spacing between patterns. SRAFs can be added whenever a poly line is sufficiently isolated, but a certain minimum assist-to-poly and assist-to-assist spacings are required to prevent SRAFs from printing space[12]. If the assist feature insertion is not considered during layout, sizing of assist feature and adjustment of exposure dose must be applied. This will cause problems in mask inspection as well as CD degradation. For instance, smaller SRAFs make mask inspection difficult and require higher-resolution inspection tools.

[1]The Bossung plot shows multiple CD versus defocus curves at different exposure doses, and has been a useful tool to evaluate lithographic manufacturability. The common process window between dense and isolated patterns is an increasingly important requirement to maintain CD tolerances in the subwavelength lithography regime.

[2]Process window is defined as the range of exposure dose and defocus within which acceptable CD tolerance is maintained.

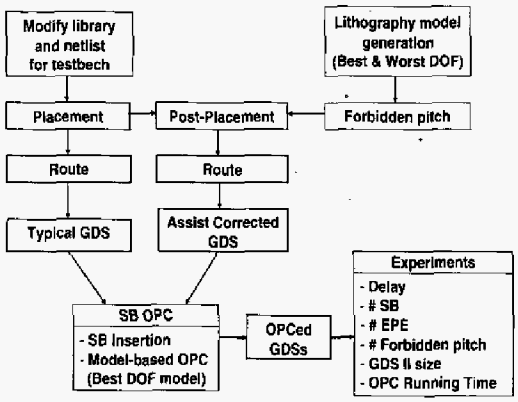

Fig. 2. The modified design and evaluation flows: Note the added steps of forbidden pitch extraction and post-placement optimization to ASIC design flow

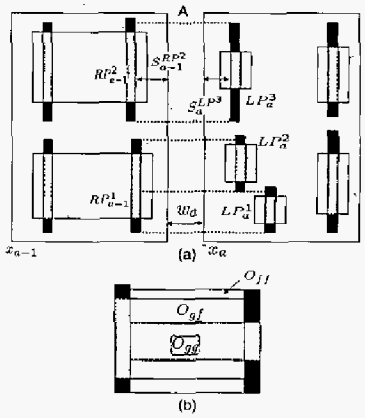

Fig. 3. (a) Multiple interactions of gate-to-gate, gate-to-field, and field-to-gate, and (b) overlapped area in the region A of (a).

III. Assist Feature Correction Methodology

A. Modified Design and Evaluation Flow

To account for new geometric constraints that arise due to SRAF OPC in physical design, we add forbidden pitch extraction and post-placement optimization into the current ASIC design methodology. Figure 2 shows the modified design and evaluation flows in the regime of forbidden pitch restrictions. Of course, we must assume that the library cells themselves have been laid out with awareness of forbidden pitches, and indeed our experiments with commercial libraries confirm that there are no forbidden pitch violations in poly geometries within commercial standard cells. SRAF insertion rules to enhance DOF margin are determined based on best and worst focus models.[3] Post-placement optimization generates a new placement which is more conducive to insertion of SRAFs, thus allowing a larger process window to be achieved. The two layouts generated by conventional and assist-correct flow undergo comprehensive SRAF OPC. The amount and impact of the applied RET is a function of the circuit layout. Thus we can evaluate how assist-correct placement impacts circuit performance and printability/manufacturability according to the metrics SRAF insertions and edge placement errors (EPE). The following subsections give more details of forbidden pitch extraction and its design implementation.

B. SRAF Rule and Forbidden Pitch Generation

Lack of space may prohibit insertion of a sufficient number of SRAFs, and as a result patterns may violate CD tolerance through defocus. Forbidden pitches are pitch values for which the tolerance of a given target CD is violated. Allowable pitches are all pitches other than forbidden pitches. In this subsection, we summarize the criteria for SRAF insertion and forbidden pitch extraction considering a worst-defocus model. Our SRAF insertion rule is initially generated based on the theoretical background given in [4]. Positioning of SRAFs is then adjusted based on OPC results. Large CD degradation through-pitch increases pattern bias as model-based OPC is applied, and this requires trimming of the SRAF rule to guarantee better process margin and prevent the SRAFs from printing.[4] After applying SRAF OPC with the best-focus model, test patterns are simulated with the worst-defocus model. This evaluation yields the forbidden pitches, considering maximum printability and manufacturability. The forbidden pitch rule is determined based on CD tolerance and worst defocus level, which are in turn dependent on requirements of device performance and yield. In all of the work we report here, CD tolerance is assumed to be $\pm 10\%$ of minimum line width while the worst defocus level is assumed to be $0.5\mu m$.

C. Assist Feature Correction

In this subsection, we describe the proposed AFCorr placement perturbation algorithm for assist feature correction. Single orientation polysilicon geometries are becoming common for the current and future process generations. Moreover, gates are typically laid out vertically (assuming horizontal cell rows). As a result, in the current work we consider only the horizontal forbidden pitch constraints. This allows us to treat the placement of a given cell row independent of all other rows. Therefore, in the following we describe the *single-row* AFCorr perturbation algorithm, using which the 2D AFCorr problem is solved one cell row at a time.

Given a cell C_a, let LP_a and RP_a be the sets of valid poly geometries in the cell which are located closest to the left and right outlines of the cell respectively. Only geometries with length larger than the minimum allowable length of SRAF features are considered. Define

[3] In general, the best focus is shifted from zero to about $0.1\mu m$ due to refraction in the resist. The worst defocus is the maximum allowable defocus corner for manufacturability in a lithography system.

[4] More complicated approaches to SRAF rule generation may involve co-optimization of model-based OPC and SRAF insertion. We do not address such involved optimizations of OPC, since the focus of our work is OPC-aware design and not OPC itself.

$s_a^{LP^i}$ to be the space between the left outline of the cell and the i^{th} left border poly geometry. Also assume a set $AF = AF_1, \ldots, AF_m$ of spacings which are "assist-correct", i.e., if the spacing between two gate poly shapes belongs to the set AF, then the required number of assist features can be inserted between the two poly geometries. AF_j denotes the j^{th} member of the set of assist-feature correct spacings AF when AF is assumed to be sorted in increasing order. Note that the set AF may contain a number of spacings which correspond to varying SRAF widths. Let w_a denote the width of cell C_a and let x_a denote its (leftmost) placement coordinate in the given standard cell row, where coordinates increase from left to right. In addition, let δ denote a cell placement perturbation to adjust the spacing between cells. Then the **assist-correct placement perturbation problem** is:

$$\text{Minimize} \sum \mid \delta_i \mid$$

$$\delta_{a+1} + x_{a+1} - x_a - \delta_a - w_a + s_{a+1}^{LP^k} + s_a^{RP^g} \in AS$$

$$\text{s.t. } LP^k \text{ and } RP^g \text{ overlap}$$

The objective can be made aware of cells in critical paths by a weighting function. Since the available number of allowable spacings is very small, obtaining a completely assist-correct solution is usually not possible in a fixed cell row width context. Therefore, a more tractable objective is to minimize the expected CD error at a predetermined defocus level. We solve this "continuous" version of the above problem with the following dynamic programming recurrence.

$$Cost(1, b) = \mid x_1 - b \mid$$

$$Cost(a, b) = \lambda(a) \mid (x_a - b) \mid +$$

$$Min_{i=x_{a-1}-SRCH}^{x_{a-1}+SRCH} \{Cost(a-1, i) + HCost(a, b, a-1, i)\}$$

$Cost(a, b)$ is the cost of placing cell a at placement site number b. The cells and the placement sites are indexed from left to right in the standard cell row. We restrict the perturbation of any cell to $\pm SRCH$ placement sites from its initial location. This helps contain the delay and runtime overheads of AFCorr placement post-processing. λ is a factor which decides the relative importance of preserving the initial placement and the final AFCorr benefit achieved for each given cell instance; in the current implementation, λ is directly proportional to the number of critical timing paths that pass through the given cell instance. *HCost* corresponds to the printability deterioration under defocus conditions for the vertically oriented poly geometries closest to the cell boundary, and depends on the difference between the current nearest-neighbor spacing of the polys and the closest assist-feature correct spacing. The method of computing *HCost* is shown in Figure 4. O_{gg}, O_{ff} and O_{gf} correspond to the length of overlapped area in the cases of gate-to-gate, field-to-field and gate-to-field poly as shown in Figure 3. In addition, c_{gg}, c_{ff}, and c_{gf} are proportionality factors which specify the relative importance of printability for gate and field poly. Typically, gate poly geometries need to be

HCost(a,b,a-1,i) of Cell C_a

Input:
User-defined weight for overlapping field polys : c_{ff}
User-defined weight for overlapping gate polys : c_{gg}
User-defined weight for overlapping gate and field polys : c_{gf}
Origin x (left) coordinate and length of cell $C_a = b$
Origin x (left) coordinate and length of cell $C_{a-1} = i$
Width of cell $C_a = w_a$
Width of cell $C_{a-1} = w_{a-1}$

Output:
Value of *HCost*

Algorithm:
01.**Case** $a = 1$: $HCost(1; b) = 0$
02.**Case** $a > 1$ **Do**
03. N:= cardinality of the set RP_{a-1}
04. M:= cardinality of the set LP_a
05. **For** $(k = 1 \; ; \; k = N \; ; \; k = k + 1)\{$
06. **For** $(g = 1 \; ; \; g = M \; ; \; g = g + 1)$ {
Let $Hspace(k, g)$ denote the horizontal spacing between RP_{a-1}^k and let LP_a^g. $O_{ff}(k, g)$, $O_{fg}(k, g)$ and $O_{gg}(k, g)$ denote the field-to-field, field-to-gate and gate-to-gate overlap lengths between RP_{a-1}^k and LP_a^g. Then $slope(j)$ is the degradation of CD with respect to pitch when spacing between two poly geometries is between AF_j and AF_{j+1}.
/* Calculate overlap weight between RP_a^k and LP_{a-1}^g */
07. $weight(g, k) = slope(j) \times (Hspace(k, g) - AF_j)$
$\times (c_{ff} O_{ff}(k, g) + c_{gf} O_{gf}(k, g) + c_{gg} O_{gg}(k, g))$
s.t. $AF_{j+1} > Hspace(k, g) \geq AF_j$,
08. $Hcost(a, b, a-1, i)$ += $weight(g, k)$
}
}

Fig. 4. The algorithm of horizontal Cost, *HCost*, calculation.

better controlled through process as they have been direct impact on performance. Therefore, a typical order is $c_{gg} \geq c_{fg} \geq c_{ff}$. Finally $slope(j)$ is defined as delta CD difference over delta pitch between AF_j and AF_{j+1}. Thus, perturbation cost is a function of *slope*, length and weight of overlapped polys, and space for SRAF insertion. Our algorithm takes a legal placement as an input, and outputs a legal placement with better depth of focus properties. The calculation time of *HCost* highly depends on N and M which are less then 3 in the standard cell designs. The runtime of the AFCorr algorithm is $O(ncell \times SRCH)$, where *ncell* is the total number of cells in the design.

IV. Experiments and Discussion

A. Experimental Setup

We synthesize the *alu*128 benchmark design from *Opencores* in *Artisan TSMC 0.13μm* and *Artisan TSMC 0.09μm* libraries using *Synopsys Design Compiler v2003.06-SP1*. *alu*128 synthesizes to 13279 cells and 8722 cells in 130nm and 90nm technologies, respectively. The synthesized netlists are placed with row utilization ranging from 50% to 90% using *Cadence First Encounter v3.3*. All designs are trial routed before running timing analysis. On the lithography side, we use *KLA-Tencor Prolith* to generate models for OPC. *Mentor Graphics Calibre* is used for model-based OPC, SRAF OPC and optical rule checking (ORC). Simulation is performed with wavelength λ = 248nm and numerical aperture NA = 0.6 for 130nm and λ = 193nm and NA = 0.75 for 90nm. An annular aperture with $\sigma = 0.85/0.65$ is used for both processes.

Proximity plots with fixed line width of $0.13\mu m$ are illustrated in Figure 5. Exposure dose focuses on the

	$0.13\mu m$ Lithography		$0.09\mu m$ Lithography	
	Pitch($X : \mu m$)	Slope	Pitch($X : \mu m$)	Slope
#SRAF = 0	$0 \leq X < 0.51$	0.28	$0 \leq X < 0.41$	0.162
#SRAF = 1	$0.51 \leq X < 0.73$	0.22	$0.41 \leq X < 0.57$	0.075
#SRAF = 2	$0.73 \leq X < 0.95$	0.105	$0.57 \leq X < 0.73$	0.062
#SRAF = 3	$0.95 \leq X < 1.17$	0.07	$0.73 \leq X < 0.89$	0.050
#SRAF = 4	$1.17 \leq X$	0.02	$0.89 \leq X$	0.012

TABLE I
SRAF RULE TABLE IN $0.13\mu m$ AND $0.09\mu m$ LITHOGRAPHY.

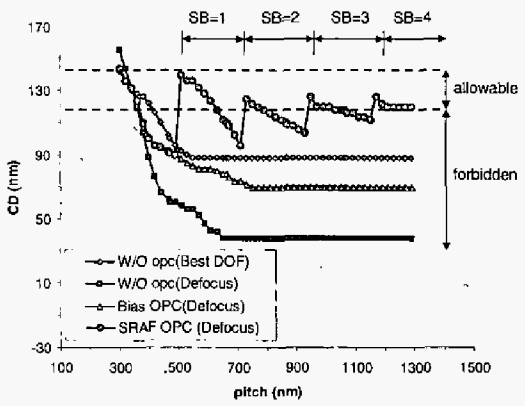

Fig. 5. Evaluation of proximity plots in through-pitch: Best focus without OPC, worst defocus without OPC, worst defocus with BIAS OPC, and worst defocus with SRAF OPC.

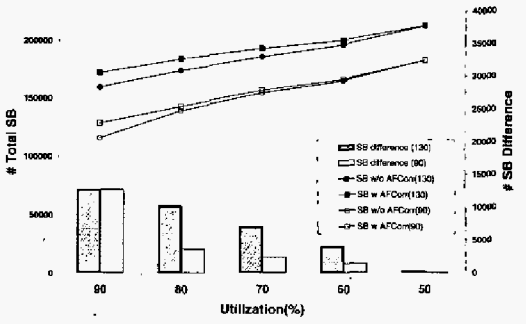

Fig. 6. Number of SRAFs with and without AFCorr for each of five different utilizations.

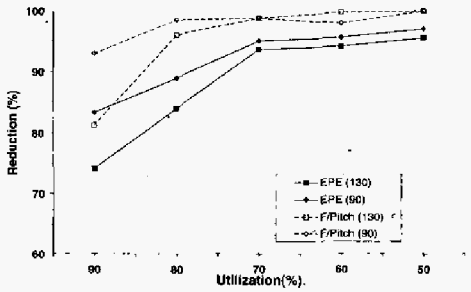

Fig. 7. Reductions of EPE and forbidden pitches with and without AFCorr for each of five different utilizations.

pattern in the minimum pitch of $0.13\mu m$. CD degradation increases through-pitch as the defocus level increases. Patterns in the pitches of over $0.4\mu m$ before OPC are outside the allowable tolerance range at the worst defocus of $0.5\mu m$. After bias OPC, pitches up to $0.38\mu m$ are allowable for CD tolerance while all pitches larger than than $0.38\mu m$ should be forbidden. After evaluating SRAF OPC patterns with the worst defocus model, a set of forbidden pitches is obtained as follows: [0.37, 0.509], [0.635, 0.729], [0.82, 0.949], and [1.09, 1.169] (microns). Forbidden pitches still remain after SRAF OPC even though OPC considerably reduces forbidden pitches in comparison to bias OPC. We generate SRAF rules based on the criteria mentioned above, with results in Table I. SRAF width is 60nm for 130nm and 40nm for 90nm technology.

B. Experimental Results

The post-placement optimization is performed based on forbidden pitches and slopes of CD error within them. After AFCorr placement perturbation, we obtain a new placement wherein the coordinates of cells have been adjusted to avoid the forbidden pitches. We use three printability quality metrics. *Forbidden Pitch Count* is the number of border poly geometries estimated as having greater than 10% CD error through-focus. *EPE Count* is the number of edge fragments on border poly geometries having greater than 10% edge placement error at the worst defocus level. This is estimated by ORC. *SB Count* is the total number of scattering bars or SRAFs inserted in the design. A higher number of SRAFs indicates less through-focus variation and is hence desirable.

We use $c_{fg} = c_{gg} = c_{ff} = 0.33$, $\lambda(a) = \frac{sitewidth}{10} \times$ (number of top 200 critical paths passing through cell a) and $SRCH = 5$.

Figure 6 shows that the total number of SRAFs increases as the utilization decreases, due to increased whitespace between cells. The benefit of the AFCorr decreases with lower utilization because the design already has enough whitespace for SRAF insertion. Due to the additional number of SRAFs inserted there is a small increase in SRAF OPC runtime (< 3.6%) and final data volume (< 3%). Reductions of EPE and forbidden pitch are investigated for each utilization as shown in Figure 7. Forbidden Pitch Count is reduced by 81%-100% in 130nm and 93%-100% in 90nm. EPE Count is reduced by 74%-95% in 130nm and 83%-96% in 90nm. In addition, SB Count improves by 0.1%-7.4% for 130nm and 0%-7.9% for 90nm. Note that these numbers are small as they correspond to the entire layout rather than just the border poly geometries. The change in estimated post-trial route circuit delay ranges from -7% to +11%. All of these results are summarized in Table II.

	Utilization (%):	90		80		70		60		50	
	Flow:	Typical	AFCorr	Typical	AFCorr	Typical	AFCorr	Typical	AFCorr	Typical	AFCorr
130nm	# Forbidden	10329	1936	6599	267	4032	51	2266	5	181	0
	# SB	158987	171691	173673	183860	185493	192578	195741	199704	212079	212412
	# EPE	8772	2267	5975	962	4276	274	1732	101	199	9
	Runtime (s)	6721	6732	6839	6899	6878	6923	6943	6944	7032	7039
	GDS (MB)	42.9	41.9	41.8	42.3	42.2	42.2	44.9	44.9	45.2	45.4
	Delay (ns)	4.21	4.49	4.547	4.444	4.501	4.372	5.142	4.976	5.051	4.942
90nm	# Forbidden	7795	545	4945	75	2753	34	1488	31	57	0
	# SB	115652	128387	139182	14752	153904	156244	164264	165649	182572	182666
	# EPE	7523	1262	4813	532	2131	107	1329	59	163	5
	Runtime (s)	4835	5011	5451	5535	5529	5632	5685	5698	5943	5944
	GDS (MB)	41.1	42.3	41.2	43.2	42.2	42.3	42.9	42.8	43.6	43.6
	Delay (ns)	2.478	2.305	2.458	2.602	2.522	2.47	2.867	3.176	3.113	3.046

TABLE II

SUMMARY OF AFCORR RESULTS. RUNTIME DENOTES THE RUNTIME OF SRAF INSERTION AND MODEL-BASED OPC. THE AFCORR. PERTURBATION RUNTIME RANGES FROM 2 TO 3 MINUTES FOR ALL TEST CASES. GDS SIZE IS THE POST-SRAF OPC DATA VOLUME.

V. CONCLUSIONS AND ONGOING WORK

In this work, we have presented a novel placement-perturbation technique, called AFCorr, as a practical and effective approach to achieve assist feature compatibility in physical layouts. AFCorr leads to reduced CD variation and enhanced DOF margin. AFCorr placement perturbation can achieve up to 100% reduction in number of cell border poly geometries having forbidden pitch violations. The corresponding reduction in large edge placement errors is up to 100%. We also achieve up to 7.9% increase in the number of inserted scattering bars. The increases of data size, OPC running time and maximum delay overheads of AFCorr are within 3%, 4% and 11% respectively. The runtime of AFCorr placement perturbation is negligible ($\sim$ 3 minutes) compared to the running time of OPC ($\sim$ 2 hours).

We are currently engaged in further experimental validation and research. For example, we would like to confirm the EPE sensitivity improvement expected by AFCorr. Our ongoing research is in the following directions:

- Pattern bridge between field poly geometries is a major reason for yield degradation even though CD variation of gates determines circuit performance. Extensions to AFCorr to account for interactions between adjacent cell rows are under investigation.
- Restricted design rules are gaining support in the industry. Part of our ongoing work analyzes "correct-by-construction" standard-cell layouts which are always AFCorrect in any placement scenario. We intend to compare such an approach with AFCorr placement perturbation in terms of design as well as manufacturability metrics.
- As AFCorr only affects inter-cell forbidden pitches, its benefit would be larger for designs using smaller sized cells. We intend to further study this dependence by analyzing a variety of testcase designs.
- Certain devices and cells may be able to tolerate more process variation than others in the design. We are investigating techniques to bias the AFCorr solution in favor of such devices to reduce timing and power impact and increase overal parametric yield.
- We are verifying greater advantages of AFCorr that are expected in future technology nodes, e.g., extensions to phase-shift mask cell "composability" and etch dummy optimization.

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