Defect Avoidance for Extreme Ultraviolet Mask Defects using Intentional Pattern Deformation

Yoo-Jin Chae[a], Rik Jonckheere[b], Puneet Gupta[a]

[a]Electrical and Computer Engineering Department, University of California, Los Angeles; [b]IMEC, Leuven, Belgium

(puneetg@ucla.edu)

ABSTRACT

Extreme ultraviolet lithography has been adopted as the next generation lithography solution to sub 10nm technology node. However, mask blank defect is a major challenge for this technology. In this work, we explore the extended benefits of utilizing pattern deformation for EUV mask defect avoidance. In the first part of the paper, we propose a constraint programming based method that can explore pattern shift, small angle rotation, and deformation for defect avoidance. In the second part of the paper, we utilized this proposed method to explore the benefit of pattern deformation. For an 8nm polysilicon layer of an ARM Cortex M0 layout, pattern deformation combined with pattern shift was able to improve mask yield by more than 90%-point compared to pattern shift alone for a 40-defect mask.

Keywords: EUV lithography, mask blank defects, defect avoidance, pattern deformation

1. INTRODUCTION

Lithography is the key technology to the next scaled node. Optical lithography has been used for semiconductor manufacturing as it is a reliable and economical mechanism for mass production. Currently, deep ultraviolet (DUV) lithography with 193nm wavelength is being used for mass production. However, it is becoming more difficult to achieve the necessary resolution needed for sub-10nm technology node with DUV. Thus, extreme ultraviolet (EUV) lithography, using 13.5nm wavelength, has gained traction to be the next generation lithography [1]. Despite the maturity of the industry for this technology, mass production of sub-10nm is still a challenge. Especially, EUV mask defect is a serious bottleneck for the advancement of this technology to mass production.

Much efforts have been devoted into developing techniques and methods to repair mask blank defects. Post-mask write repair methods such as absorber removal and deposit/etch of multilayer are methods that physically target the defects [2]. Although these repair methods are available, there is a significant risk of damaging the structure of the mask since the defects are buried under multilayers [3]. Pre-mask write methods, however, utilizes absorber patterns to minimize the impact of defect on printings on silicon wafer. It has been found that aligning the absorber pattern with the defect can mitigate the impact of defect on CD [4]. We can either choose to hide the defect under the absorber pattern or place them far away from absorber edges such that reflectivity around the pattern edges is not compromised. Figure 1 shows the flow of pre-mask write defect avoidance method.

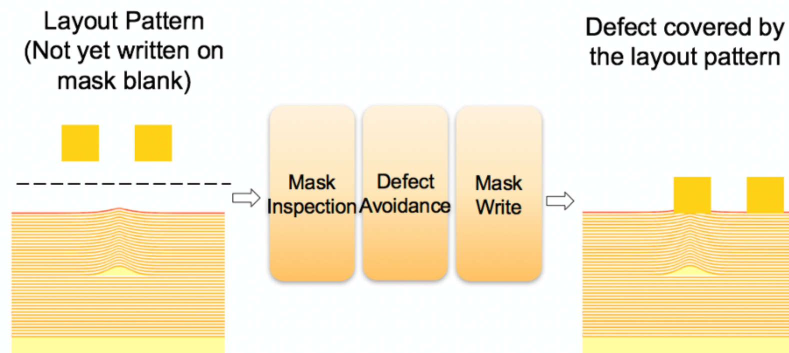

Figure 1: Pre-mask write defect avoidance flow

In order to mitigate the defects, we must compute an optimal alignment value that accommodates for the location of the defects on each mask blank. In this paper, we explore combination of the following degrees of freedom to find the optimal solution for defect avoidance:

- Pattern Shift: Absorber pattern is shifted in *x* and *y* direction relative to the mask blank. The benefits of pattern shift methods of implementation have been explored and developed by several prior studies [4] [5] [6].
- Small Angle Rotation: Absorber pattern is rotated around the center of the mask. It was proposed by Zhang et. al. [8] and explored by several prior studies [7] [9].
- Pattern deformation: Absorber pattern is intentionally deformed by magnification and/or high-order deformation then later corrected in process of printing on silicon wafer using scanner operations. The concept of high-order deformation was suggested by Jonckheere as a form of intentional pattern deformation [10]. Second-order deformation is subset of pattern deformation where the mask pattern is deformed in a bow shape as shown in Figure 2.

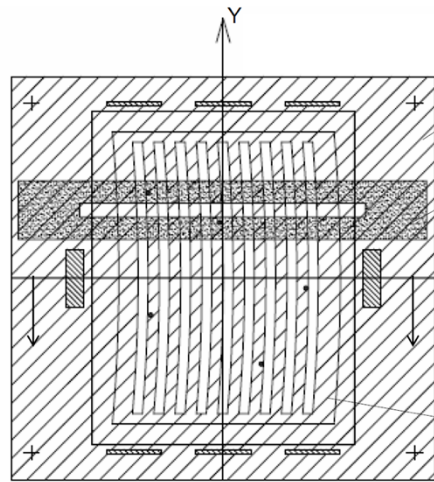

Figure 2: Example of intentional pattern deformation. The mask pattern in the field area, here containing vertical lines and spaces, is deformed by a bow as example of non-linear deformation. [10]

Figure 3 shows summary example of conceptual benefit for defect avoidance using the given degrees of freedom.

Figure 3: Summary example showing benefit of pattern deformation

In this paper, we utilize this defect avoidance method to further investigate the benefit of mask defect mitigation using intentional pattern deformation as added degree of freedom to previous works. Previous studies have looked at pattern shift, rotation, and mask floorplanning as part of their degree of freedom [7]. In this paper, we study the feasibility and

added benefit of pattern deformation for defect avoidance, by selected sub-aspects – magnification and second order deformation.

The key contribution of this paper are as follows:

- We explore the benefit of intentional pattern deformation for defect avoidance.
- We developed a constraint programming based methodology to compute optimal values for degrees of freedom – pattern shift, rotation and high-order deformation.

This paper is organized as follows. Section 2 outlines the algorithm and methodology developed to explore the benefit of intentional pattern deformation. Section 3 describes the experimental setup and results using the developed method. It also shows the validation of these results using prohibited region method, and concludes the paper.

2. PROPOSED CONSTRAINT PROGRAMMING METHOD

There have been several prior studies that looked at methods to exploit defect avoidance. Zhang et al. proposed a prohibited region method that constructs regions around the edges where defects cannot be placed as shown in Figure 4 [5]. This methodology creates a geometric map of locations where the defects cannot be placed, then this geometric map is used to formulate the minimum rectangle overlapping problem which can efficiently compute for available shift for all defects. While this method is efficient in computing pattern shift, it cannot accommodate for pattern deformation as part of its degree of freedom. Thus, we need a novel approach which considers pattern deformation as well. In this section, we propose a constraint programming based method to consider the added degree of freedom and explore its benefits.

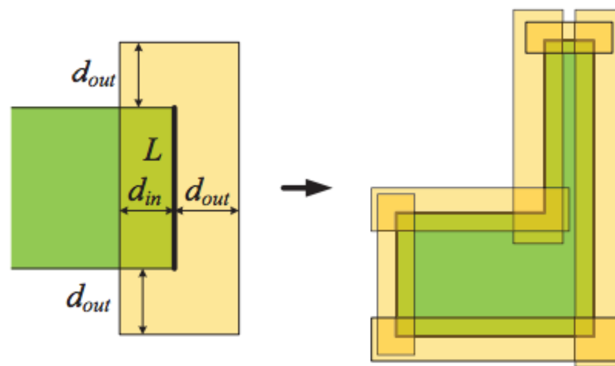

Figure 4: Definition of prohibited region [5]

2.1 Modeling Pattern Deformation as Shift in Defect Location

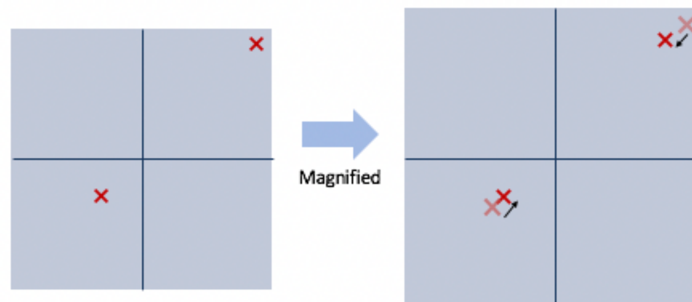

Figure 6: Modeling magnification as a local shift in relative defect locations to absorber pattern

Figure 6 shows how positive magnification of the absorber pattern can be seen as a local shift in relative defect locations toward the origin. The relative shift is in opposite orientation to the magnification, thus the shift is modeled as an inverse

of magnification to defect locations. New defect location can be written as $(\alpha_x \cdot x_{dn},\ \alpha_y \cdot y_{dn})$ where $(x_{dn},\ y_{dn})$ is the location of the original n^{th} defect, and (α_x, α_y) is the inverse of $(mag_x,\ mag_y)$.

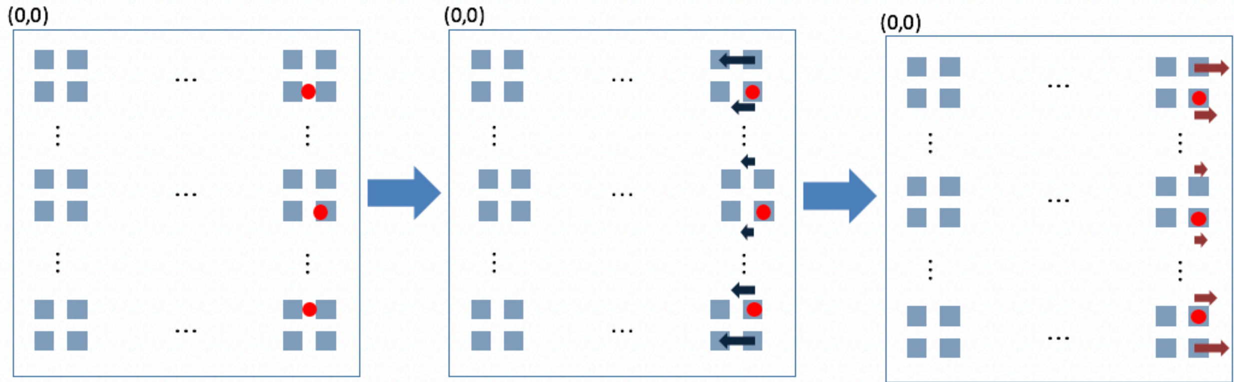

Figure 7: Modeling second order deformation as a local shift in relative defect location to absorber pattern

The same idea can be applied to second order deformation. The new relative location of the defect to absorber pattern is modeled as a local shift in the opposite direction of the second order deformation as shown in Figure 7. The new defect location can be written as $(x_{dn} - \beta_x \cdot y_{dn}^2,\ y_{dn} - \beta_y \cdot x_{dn}^2)$ where β is the second order deformation constant.

Magnification has two impacts on the absorber patterns – it changes the location of each polygon and magnifies the size of each polygon (shown in Figure 8). However, only the change in locations is taken into consideration in our problem formulation. An assumption is made that the magnification does not affect the size of the polygons.

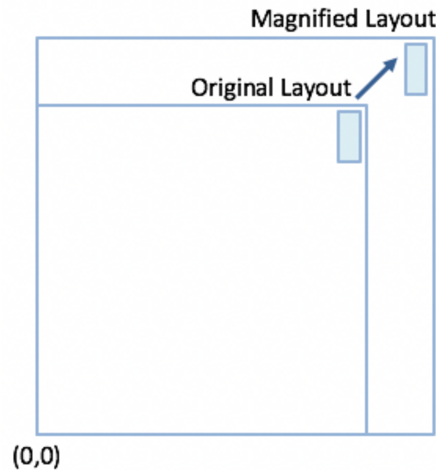

Figure 8: Impact of magnification on the absorber patterns

This assumption is valid for a very small magnification value. For instance, each polysilicon polygon in ARM Cortex M0 has width of 300 dbu (=30nm) and length of 15,000 dbu (=1500nm). We use 0.1% magnification to enlarge each polygon size to 300 × 15002 dbu. The width does not change as they round down to the nearest integer with small magnification value. Length changes by 2 dbu, however, this is acceptable as the difference in value is less within the safety margin (=20nm) of our prohibited region calculation. To confirm that our assumption was valid, we used prohibited region method as shown in Figure 4 implemented with C++ using OpenAccess [11] and Boost Polygon [12] to magnify the design and verify the results from both methods were identical.

2.2 Constraint Programming Method Problem Formulation

We formulate a constraint programming based model for our defect avoidance for EUV mask defects. Our framework takes inputs of defect location, prohibited regions, and ranges of allowed degree of freedom. Then, returns the maximum number of mitigated defects and corresponding degrees of freedom values. In the following, we use notations as described in Table 1.

Table 1: Notations

Notation	Meaning
$\alpha_x(\alpha_y)$	inverse of magnification in x (y) directions
$\beta_x(\beta_y)$	second order constant x (y) direction
$d_x(d_y)$	pattern shift in x (y)direction
θ	small angle rotation
$x(y)_{dn}$	x (y)coordinate of nth defect
$x(y)_{min,n}$ $x(y)_{max,n}$	minimum and maximum x (y) coordinate of prohibited regions for nth defect
$x(y)_{rot}$	x (y) coordinate of rotated defect location
$new_x(y)_{dn}$	x (y) coordinate of new defect location

There are constraints that must be satisfied to ensure the manufacturability of the final mask. They limit the degrees of freedom and are dependent on: 1. size of the usable area of the mask compared to entire mask field size, 2. capability of the lithography tools to correct for deformation, 3. accuracy of lithography tools that determines the resolution for degrees of freedom. These translate to mathematical constraints in problem formation which is outlined as constraints (2), (3), (4) and (5).

$$\textbf{Find} \quad \{\alpha_x, \alpha_y, d_x, d_y, \beta_x, \beta_y, \theta\} \tag{1}$$

$$\textbf{so that} \quad \frac{1}{mag_{max}} \le a_{x,y} \le \frac{1}{mag_{min}} \tag{2}$$

$$shift_{min} \le d_{x,y} \le shift_{max} \tag{3}$$

$$\beta_{min} \le \beta_{x,y} \le \beta_{max} \tag{4}$$

$$\theta_{min} \le \theta \le \theta_{max} \tag{5}$$

$$\sum_n x_{min,n} \le new_x_{dn} \le x_{max,n} \ \& \ y_{min,n} \le new_y_{dn} \le y_{max,n} = 0 \tag{6}$$

Equations (1) through (6) define the model. The objective function (1) represents the finding degrees of freedom for defect avoidance. Constraint (2), (3), (4), and (5) defines the range of allowed degree of freedom. Constraint (6) defines the illegal solution space for new defect locations. The rotated and new defect location is written as following:

$$(new_x_{dn},\ new_y_{dn}) = (\alpha_x x_{rot} - \beta_x y_{rot}^2 - d_x,\ \alpha_y y_{rot} - \beta_y x_{rot}^2 - d_y) \tag{7}$$

$$(x_{rot},\ y_{rot}) = (x_{dn}(1 - \frac{\theta^2}{2}) - y_{dn}\theta,\ \ y_{dn}(1 - \frac{\theta^2}{2}) - x_{dn}\theta) \tag{8}$$

Figure 9 demonstrates illegal (prohibited region) and legal solution space for a defect. Each illegal solution space (denoted as ① and ② in Figure 9) is added to the model as described in constraint (6) which prohibits the new defect location to be placed in such space.

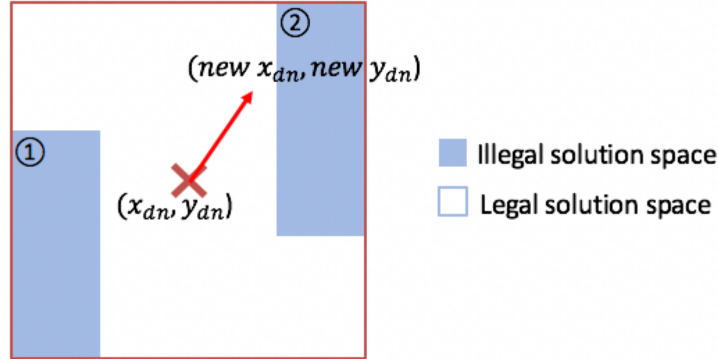

Figure 9: Example of defect location and its surrounding solution space

Our proposed method returns the maximum number of defects covered by the given degrees of freedom and solution space. This is achieved by returning the number of defects when the model becomes infeasible to solve. Since the constraint for each defect is added in the order of the data written in the program, the number of mitigated defects are order dependent. However, this dependency is acceptable since imec_n7 defect map was ordered from high priority to low priority. For ARM Cortex M0, 100 defect maps were randomly generated for Monte Carlo analysis which are further discussed in Section 3.

3. RESULTS AND DISCUSSION

3.1 Experimental Setup

Our proposed constraint programming based EUV mask defect avoidance method has been implemented in Python using Decision Optimization CPLEX API developed by IBM [13]. We chose to use constraint programming as our method of choice because it is efficient in handling logical constraints and it allows us to explore all solution spaces (unlike other mathematical programming methods where object function is needed). Our solutions from constraint programming method were validated using prohibited region to ensure the assumptions made in our methods were valid. To do so, we implemented prohibited region method in C++ using OpenAccess and Boost Polygon API. OpenAccess was used to read and deform the layout shapes, then Boost Polygon API was used to perform polygon Boolean operations.

We used ARM Cortex M0 processor layout and a 7nm technology node inspired test design provided by imec (referred to as imec_n7). ARM Cortex M0 was synthesized, placed and routed using Cadence Encounter with 32 nm Synopsys Standard Cell Library [14]. The layout was then scaled to an 8nm technology node for our experiment. ARM Cortex M0 layout is $162 \times 159\ \mu m^2$ and imec_n7 layout is $152 \times 152\ \mu m^2$. Note that these die sizes are much smaller than the full-field size of masks. The defect density used in our analysis, much higher than typical, may not represent the realistic values in production. Nonetheless, the selected test cases are fully appropriate to evaluate the effectiveness of our proposed method.

On the ARM Cortex M0 design, Monte Carlo analysis over a 100 random defect map was performed to determine the effectiveness of our method. 100 random spatial defect maps were generated to test our method and it was assumed that the defects were distributed uniformly across the mask. Each map consisted of 50 defects and our constraint programming method returned the maximum number of defects that could be avoided. Mask yield shown in these results are percentage of defect maps that are made usable (no impact on chip yield) through defect avoidance.

On imec_n7 design, we used a single defect map of 57 defect count provided by imec. The number of mitigated defects by our methodology are listed for this design as the defect coverage yield.

In creating the prohibited rectangles, we set the "safety margin" to be 20nm for all our designs. Safety margin refers to the distance the defect must be placed to not affect the printing on the wafer (noted as d_{in} and d_{out} in Figure 4). It accounts for the lateral defect size as well as location uncertainties of the defects. We allow a maximum pattern shift of 20µm, a small-angle rotation of 3° and magnification of 0.1%. Maximum second-order deformation term β is 10 ppb for our designs, as the deformed pattern displacement due to $\beta_x y_{dn}^2$ term should not exceed certain limit.

3.2 Experimental Results

Table 2: Summary of mask yield of ARM Cortex M0 layers using 20µm pattern shift

Defect Count	POLY	M1	ACT	CO
10	100%	100%	100%	100%
20	100%	100%	100%	100%
30	44%	100%	100%	100%
40	5%	100%	100%	100%
50	0%	86%	100%	100%

Table 2 shows mask yield using only pattern shift for four critical layers for EUV. As shown, 20µm pattern shift is a sufficient degree of freedom for defect avoidance for metal 1, active and contact layers. However, 20µm pattern shift is not a sufficient degree of freedom for polysilicon layers which has unidirectional and equally spaced parallel shapes. Thus, the further degree of freedom is necessary for polysilicon layer and is the subject of our study. The following results for ARM Cortex M0 design are for polysilicon layer.

Table 3: Summary of mask yield of ARM Cortex M0 polysilicon layer after using our defect avoidance method

Defect Count	Shift	Shift + rotation	Shift + magnification	Shift + magnification + 2nd order deformation	Shift + rotation + magnification
10	100%	100%	100%	100%	100%
20	100%	100%	100%	100%	100%
30	44%	100%	100%	100%	100%
40	5%	29%	53%	100%	98%
50	0%	0%	9%	51%	26%

Table 3 shows the summary of our mask yield for polysilicon layer on ARM Cortex M0 design. We see a major improvement for yield in defect maps with 30, 40, 50 counts. While shift can only mitigate 44% of the defect maps for 30, adding another degree of freedom such as rotation and/or magnification allows the yield to become 100%. For defect count maps with 50 counts, combination of magnification and second order deformation was able to achieve 51%, compared at 0% yield solely using pattern shift.

These results show that non-linear degrees of freedom when combined with pattern shift benefit defect avoidance. This is because defect avoidance by linear degree of freedom, such as pattern shift, is limited by regular and unidirectional polysilicon layer.

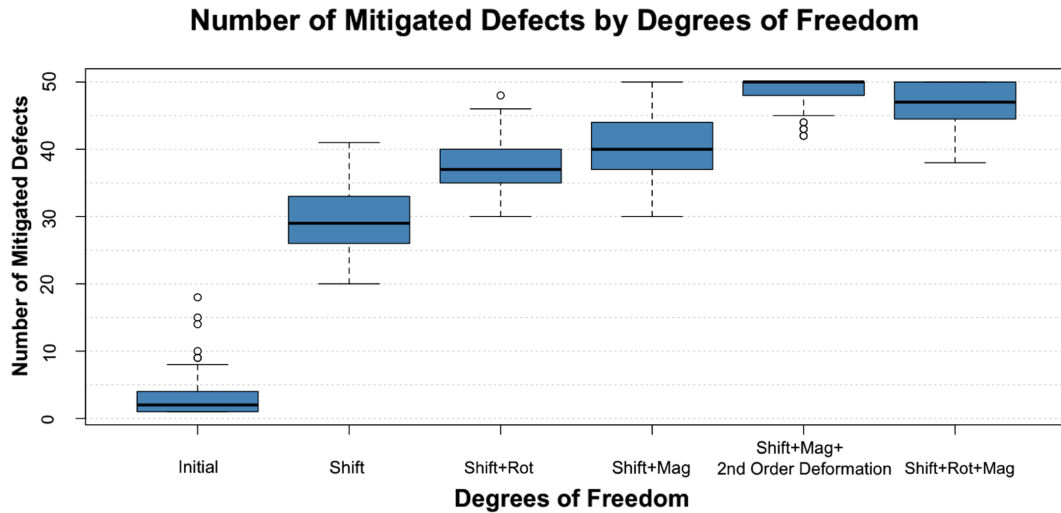

Figure 10: Boxplot of number of defects mitigated in polysilicon layer by degrees of freedom

Our constraint programming method returns the maximum number of defects mitigated. Figure 10 shows a boxplot of number of mitigated defects in polysilicon layer by degrees of freedom. The results show that combination of shift, magnification and second order deformation is the most effective degree of freedom for the polysilicon layer. It yields the highest number of mitigated defects with the average of 48.4 and median of 50 defects as shown in Table 4. These specific results pertain to the ARM Cortex M0 polysilicon layer and different combinations of degree of freedom may be more suitable for different designs.

Table 4: Average and median number of defects mitigated in polysilicon layer by degrees of freedom

	Initial	Shift	Shift + rotation	Shift + magnification	Shift + magnification + 2nd order deformation	Shift + rotation + magnification
Average	3.3	29.4	37.5	40.5	48.4	46.5
Median	2	29	37	40	50	47

We tested the combination of degrees of freedom on two layers of imec_n7 design – via 1 layer (M20-V1) and metal 2 layer (M30-M2). Table 5 shows the number of mitigated defects from the provided defect map. In via 1 layer, combination of shift, magnification and second order deformation can avoid up to 17 more defects compared to only pattern shift. In metal 2 layer, combination of shift, magnification and rotation gives the best the improvement of 5 more mitigated defects than pattern shift.

Table 5: Number of mitigated defects in a total of 57 (% of mitigated defects) on imec_n7 design using different degrees of freedom

Degrees of Freedom	M20 – V1	M30 – M2
20u shift	36 (63.2%)	10 (17.5%)
20u shift + 0.1% mag	44 (77.2%)	13 (22.8%)

20u shift + 3° rotation	42 (73.6%)	13 (22.8%)
20u shift + 0.1% mag + 3° rotation	49 (86.0%)	15 (26.3%)
20u shift + 0.1% mag + 10ppb beta	50 (87.7%)	13 (22.8%)
20u shift + 0.1% mag + 20ppb beta	53 (93.0%)	13 (22.8%)

The difference in success for defect avoidance in via 1 and metal 2 comes from the pattern density of the layers. As pattern density increases, absorber area to cover the defect decreases making it harder to find concurrent solution space. Figure 11 illustrates the difficulties of defect coverage depending on the pattern densities. As illustrated, metal 2 has a very high pattern density, which even with additional degree of freedom it is difficult to mitigate large number of defects.

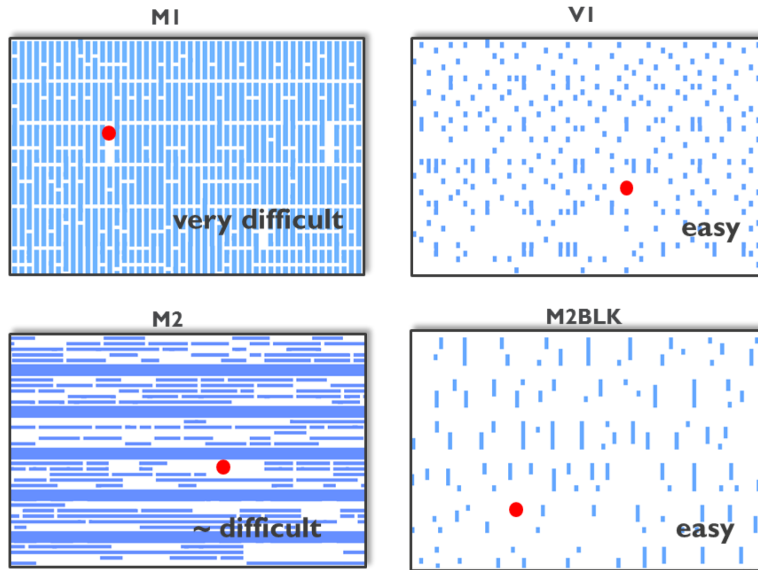

Figure 11: Illustration of defect coverage dependency on pattern density. Clear area (reflective ML) is shown in blue, and the white background represents absorber. A red dot represents a ML-defect, that is attempted to be covered by absorber [10].

3.3 Conclusion and Future Work

In this paper, we proposed an EUV mask defect avoidance method that can explore pattern shift, rotation, and pattern deformation as degrees of freedom. We modeled the degrees of freedom as displacement in relative location of defects and used constraint programming to simultaneously solve for optimal solution. Our methodology is general and allows to explore how well additional degrees of freedom provide a further benefit for defect avoidance.

Using our proposed methodology, we explored the benefits of pattern deformation as an additional degree of freedom to prior studies. Our analysis shows that pattern deformation (for our feasibility study restricted to magnification and second order deformation) can provide a significant benefit to defect avoidance under correct circumstances. For the polysilicon layer of an ARM Cortex M0 layout, pattern deformation combined with pattern shift was able to improve mask yield by more than 90%-point compared to pattern shift alone for a 40-defect mask.

Applicability and degree of possible improvement of defect avoidance method depends largely upon the ability of lithography tools to handle degrees of freedom. Pattern deformation is especially dependent since scanner operation must be modulated in order not to reproduce the pattern deformation on the wafer. Defect location uncertainty is another major bottleneck to defect avoidance. In this paper, we assume the lateral defect size and locational uncertainty is combined to be 20nm which is referred to as safety margin from absorber edges. However, if the locational uncertainty is larger, the expected mask yield may be lower.

4. ACKNOWLEDGEMENTS

Authors acknowledge the help from Dr. Yasmine Badr and Dr. Abde-Ali Kagalwalla in development of the code and for valuable discussions. This work was partly funded by the National Science Foundation and by the Center for Design-Enabled Nanofabrication (http://cden.ucsd.edu).

REFERENCES

[1] International Technology Roadmap for Semiconductors(ITRS). http://www.itrs2.net/, 2015.
[2] T. Bret, R. Jonckheere, D. Van den Heuvel, C. Baur, M. Waiblinger, G. Baralia, "Closing the gap for EUV mask repair," Proc. SPIE 8322, Extreme Ultraviolet (EUV) Lithography III, 83220C (23 March 2012)
[3] Yunfei Deng, Bruno La Fontaine, and Andrew R. Neureuther. “Performance of repaired defects and attPSM in EUV multilayer masks.” volume 4889, pp. 418–425. SPIE, 2002.
[4] John Burns and Mansoor Abbas. “EUV mask defect mitigation through pattern placement.” volume 7823, p. 782340. SPIE, 2010.
[5] H. Zhang, Y. Du, et al. “Efficient pattern relocation for EUV blank defect mitigation.” In Proc. ASP-DAC, 2012.
[6] Alfred Wagner, Martin Burkhardt, et al. “Mitigation of extreme ultraviolet mask defects by pattern shifting: Method and statistics.” J. Vac. Sci. & Technol., B, 2012.
[7] A. A. Kagalwalla and P. Gupta, “Comprehensive defect avoidance framework for mitigating extreme ultraviolet mask defects,” SPIE Journal of Micro/Nanolithography, MEMS and MOEMS (JM3), vol. 13, no. 4, p. 043005, 2014.
[8] H. Zhang, Y. Du, M. D. F. Wong, et al. Layout small-angle rotation and shift for EUV defect mitigation. In Proc. ICCAD, 2012.
[9] Ahmad Elayat, Peter Thwaite, and Steffen Schulze. “EUV mask-blank defect avoidance solutions assessment.” Proc. SPIE Photomask, 2012.
[10] Rik Jonckheere, "Overcoming EUV mask blank defects: what we can, and what we should," volume 10454, p. 104540M, SPIE, 2017.
[11] “OpenAccess API.” http://www.si2.org/.
[12] “Boost Polygon Library.” https://www.boost.org/doc/libs/release/libs/polygon/.
[13] “ILOG CPLEX Optimization Studio.” https://www.ibm.com/products/ilog-cplex-optimization-studio/.
[14] “Synopsys 32nm Library.”, 2010.