

Relaxing LER requirement in EUV lithography

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Abstract

Low throughput has been a critical issue in extreme ultraviolet (EUV) patterning due to the difficulty in increasing light source power. This limitation has driven the need for photoresists with better throughput which unfortunately come with higher line edge roughness (LER). In this work, the possibility of relaxing LER requirements for metal layer patterned by EUV lithography (EUVL) is studied. Single patterning and litho-etch litho-etch (LELE) patterning with EUVL are considered. To assess the impact of LER on design yield, analytical and simulation-based modeling approaches are developed, which consider the LER induced metal wire shorts/opens and the enhanced time-dependent dielectrics breakdown (TDDB) for metal wires with different geometries. The impact of LER on wire delay is studied by Elmore's delay model.

Keywords: EUV lithography, line edge roughness (LER), TDDB, yield estimation

1. Introduction

Due to the difficulty in increasing the power of extreme ultraviolet (EUV) light source, photoresists with high sensitivity is needed to meet the demand for high throughput. However, these photoresists usually lead to higher line edge roughness (LER). The root cause of LER in the chemically amplified photoresist is the random distribution of soluble and insoluble chemicals at the boundary of a patterned feature, which is caused by the stochastic nature of the polymer deprotection process¹⁻². Some features of EUV lithography (EUVL) also enhance LER: 1) Photons with higher energy excite secondary electrons during exposure³; 2.) the reduced light source power leads to limited exposure dose, which adds to the stochastic behavior of photons; 3). LER transferred from EUV Mask roughness³. A major factor that impacts the yield of EUVL is the LER.

At present, the metal layer is patterned by multiple patterning technology with 193nm-immersion lithography in industry. Anticipated at 5nm node, the metal layer is to be patterned by EUVL for sub-30nm interconnect pitch, which is featured by fewer exposure steps and fewer restrictions in layout design. Single patterning and litho-etch litho-etch (LELE) patterning with EUVL are two potential candidates⁴, as shown in Figure 1(a) and (b), respectively. In both of them, LER is first transferred from photoresist to hard mask during patterning and is then transferred to metal wires during the damascene process. In this paper, we assume that the line space is patterned by EUV and wires are fabricated by the damascene process.

LER can induce high yield loss and interconnect performance variability because it does not scale down with interconnect pitch. LER protrusions at wire edges can touch each other and cause short circuit, as shown in Figure 1(c). The overlay shift in the LELE patterning enhances this issue by reducing wire space. The LER at one metal wire can also cut itself off and cause open circuit, as shown in Figure 1(c). Besides, LER also enhances time-dependent dielectrics breakdown (TDDB) by reducing the local wire

space and enhancing the electrical field intensity at the protrusions. Both of these two issues can lead to catastrophic chip malfunction and increase yield loss.

Critical area based analysis has been widely used to calculate yield loss induced by photolithographic defects ⁵. In this method, the defects are usually modeled as independent random variables. However, LER is spatially correlated. Therefore, in this paper, we proposed a yield model that is based on the statistical characteristics of LER. The impact of LER on metal layer yield is evaluated by analytical and simulation-based modeling approaches, which consider LER induced metal wire shorts/opens and the enhanced TDDDB. Single patterning and LELE patterning with EUVL are considered in this study. Critical path delay variability by LER is evaluated by using Elmore's delay model. Based on these models, the yield of EUVL based metal wire patterning at 5nm node is calculated. The possibility of improving yield is explored by changing the design rules, which helps alleviate the demand for higher EUV light source power.

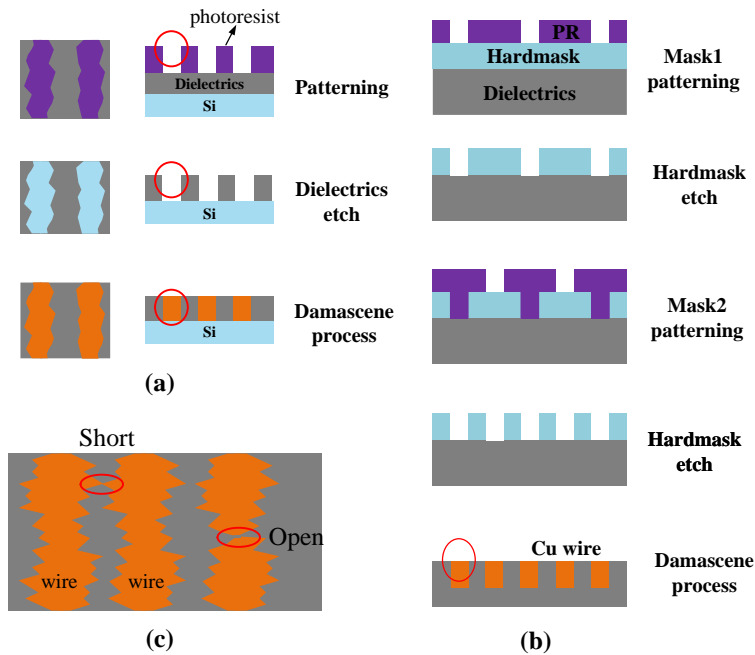


Figure 1(a) Single patterning by EUVL (b) litho-etch litho-etch patterning by EUVL (c) An illustration of wire short and open.

2. Modeling of LER Induced Failure

A. Shorts/Opens induced catastrophic failure

Wire geometry model with LER is needed to calculate shorts/opens induced catastrophic failure. A common way to generate wire geometry with LER is to conduct inverse Fourier transform from its power spectral density (PSD) with random phases, which is typically described by a Gaussian or exponential auto-correlation function ⁶. However, this method leads to a heavy computational burden for chip level estimation. In this section, a simple analytical approach is proposed, which can be applied to calculate the yield of a metal layer.

The short probability for wires with overlapping length L_N is first modeled. As shown in Figure 2, LER along the wire is sampled with interval $dx=1nm$ ⁶. $LER1=(x_{11},x_{12},\dots,x_{1i},\dots,x_{1N})$ and $LER2 =$

$(x_{21}, x_{22}, \dots, x_{2i}, \dots, x_{2N})$ are the LER magnitude along the two wires, which is defined as the deviation of actual wire edge from its original position (the dashed line). Each element in LER1 and LER2 is modeled as a Gaussian random variable with $N(0, \sigma_{LER})$, where σ_{LER} is the standard deviation of the LER magnitude. The elements in LER1 (or LER2) are spatially correlated as Eq. (1) ⁷. λ is the correlation length, which is typically 10-50nm. In this model, the metal wire is assumed to inherit the exact LER geometry from the photoresist. Wire tapering in the vertical direction and the wire thickness variation is not considered here.

$$\text{cov}(x_{ki}, x_{kj}) = \sigma_{LER}^2 \exp\left(-\left[(i-j)dx\right]^2 / \lambda^2\right) \quad (1)$$

Where $k=1$ or 2 , $1 \leq i, j \leq N$.

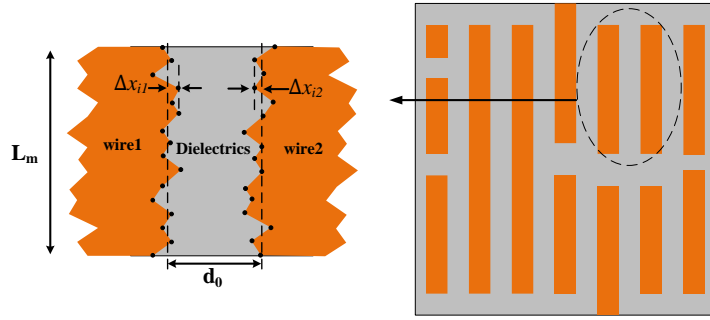


Fig. 2 An illustration of the LER model in this study

The local wire space at point i can be expressed as $d_i = d_0 - X_i$, where $X_i = x_{1i} + x_{2i}$ is with normal distribution $N(0, \sqrt{2}\sigma_{LER})$ and d_0 is the nominal wire space without LER. The spatial correlation of X can be expressed as Eq. (2) since the opposite wire edges are not spatially correlated.

$$\begin{aligned} \text{cov}(X_i, X_j) &= \text{cov}(x_{1i} + x_{2i}, x_{1j} + x_{2j}) = \text{cov}(x_{1i}, x_{1j}) + \text{cov}(x_{2i}, x_{2j}) \\ &= \left(\sqrt{2}\sigma_{LER}\right)^2 \exp\left(-\left[(i-j)dx\right]^2 / \lambda^2\right) \end{aligned} \quad (2)$$

The probability density function (PDF) of $\mathbf{x} = [X_1, X_2, X_3, \dots, X_N]^T$ is an N-dimension multivariate Gaussian distribution, as shown in Eq. (3). $\mathbf{u} = [u_1, u_2, u_3, \dots, u_n]^T$ is the vector of mean values, which is 0 here. Σ is an $N \times N$ positive definite covariance matrix and its entry is $\Sigma_{ij} = \text{Cov}(X_i, X_j)$. The cumulative probability distribution of \mathbf{x} can be calculated by the mvtnorm package in statistics software R ⁸. To reduce the dimensionality of the random variables, in this study, wires longer than $1\mu\text{m}$ are segmented into a few shorter segments that are serially connected.

$$f(\mathbf{x}) = \exp\left(-\frac{1}{2}(\mathbf{x} - \mathbf{u})^T \Sigma^{-1}(\mathbf{x} - \mathbf{u})\right) / \sqrt{(2\pi)^N \det(\Sigma)} \quad (3)$$

The wires get short circuit when LER protrusions touch each other at any point k , i.e. $X_k > d_0$. Therefore, for metal wires with length L_N , the short probability can be expressed as Eq. (4).

$$P(\text{short}, L_N) = 1 - P(X_1 < d_0, X_2 < d_0, \dots, X_N < d_0) \quad (4)$$

Similarly, the probability that a wire of length L_N gets open circuit can be expressed as Eq. (5). w_0 is the nominal wire width without LER. $Y_i = y_{1i} + y_{2i}$, where y_{1i}, y_{2i} are the LER magnitude at the two edges of a wire.

$$P(\text{open}, L_N) = 1 - P(Y_1 < w_0, Y_2 < w_0, \dots, Y_N < w_0) \quad (5)$$

In LELE patterning, the overlay shifts the spaces by u_i and the wire width becomes $w_0 - u_i$. Therefore, the open probability is expressed as Eq. (6), where the open probability under each overlay shift u_i is evaluated. The overlay shift u_i is assumed to obey normal distribution $N(0, \sigma_{\text{overlay}})$, where σ_{overlay} is the standard deviation of the overlay shift. The short probability is not affected by overlay because the space is not changed.

$$P(\text{open}, L_N) = 1 - \sum_{i=1}^m P(X_1 < w_0 - u_i, X_2 < w_0 - u_i, \dots, X_N < w_0 - u_i | u = u_i) P(u = u_i) \quad (6)$$

The open probability for a metal layer is calculated by considering all of the wires in this layer, as Eq.(7). N_{wire} is the total number of wires. The short probability in a metal layer can be calculated in a similar way by considering all the overlapping areas between metal wires.

$$P(\text{open}) = 1 - \prod_{m=1}^{N_{\text{wire}}} (1 - P(\text{open}, L_m)) \quad (7)$$

A 1D metal pattern on a $1\text{cm} \times 1\text{cm}$ chip is used to estimate the yield, as shown in Figure 3(a). The length of wire is 1cm and only 1 metal layer is considered here. Yield is defined as the probability that neither metal wire opens nor shorts occur. Note that this way may be somewhat pessimistic as it assumes a fully packed layout. We do not believe that the pessimism to be much as typical track utilization in the local metal layer is high (>75%)

Figure 3(b) shows the yield of 24nm pitch wires patterned by single patterning. The LER threshold, defined as the $3\sigma_{\text{LER}}$ value that yield reduces to 0.99, is about 3.4nm. After a narrow transition region, yield reduces to 0 at $3\sigma_{\text{LER}} = 3.8\text{nm}$, which indicates it is sensitive to $3\sigma_{\text{LER}}$ after the LER threshold. It is also observed that yield is slightly higher in the transition region by choosing a longer correlation length λ in the model. However, the LER threshold is not changed by λ . Therefore, λ is chosen to be 20nm in the rest of this paper.

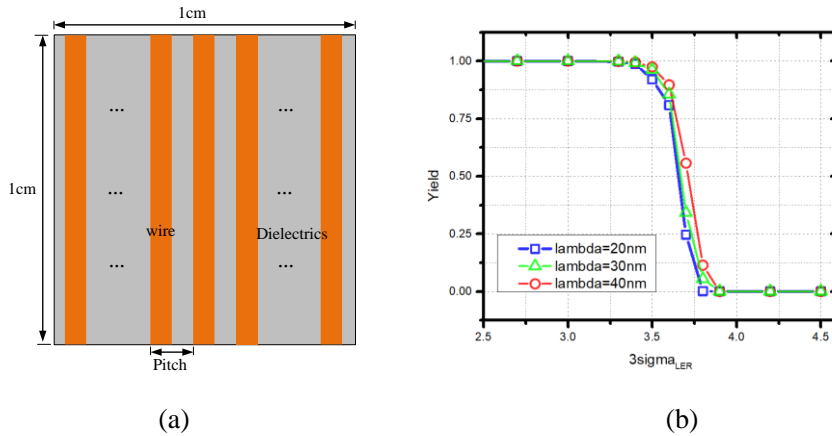


Figure 3(a) 1D metal pattern used for yield estimation. (b) The yield of 24nm pitch wires patterned by single patterning

Figure 4 presents the yield of LELE patterning under different overlay variation $3\sigma_{overlay}$. It is noticed that yield is reduced significantly as the overlay variation increases. It can be attributed to the wire width reduction by overlay shift, which leads to higher open probability. Therefore, overlay variation should be well controlled in LELE patterning to obtain a high yield. LER threshold in LELE patterning decreases to 2.4nm and 2.8nm for $3\sigma_{overlay} = 2\text{nm}$ and 3nm, respectively, which is lower than 3.4nm for single patterning. Therefore, single patterning allows higher yield with fewer restrictions on photoresist LER.

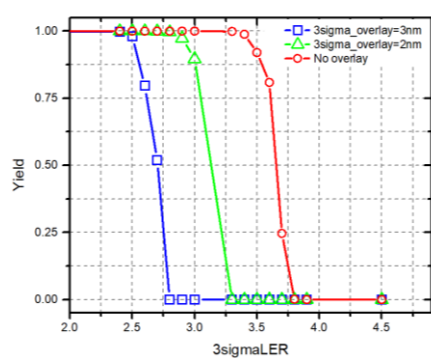


Figure 4. The yield of 24nm pitch wires patterned by LELE patterning

The yield for different wire geometries are also studied, as shown in Figure 5. Only single patterning is considered here. For 24nm pitch, three types of wires are considered: one has equal width and space (12/12nm) while the other two has larger space than width (11/13nm and 10/14nm). It is observed that the 12nm/12nm wire has higher LER threshold ($3\sigma_{LER} = 3.4\text{nm}$) than the other two cases, which is reduced to 3.1nm and less than 3nm, respectively. It can be explained by the significant increase of wire opens when its width is reduced. Besides, LER threshold is increased to about 3.9nm for 28nm pitch wire with equal width and space.

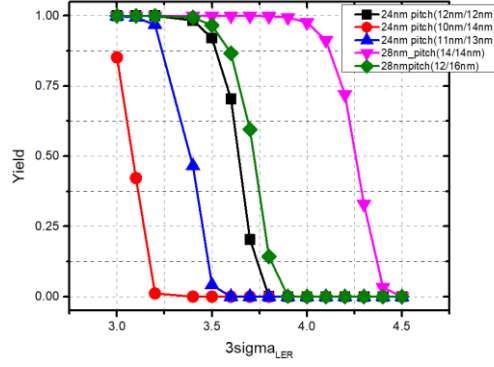


Figure 5. The yield of wires with different geometries.

B. LER enhanced time-dependent dielectrics breakdown (TDDB)

As a common reliability issue of low-k dielectrics, TDDB occurs when a conductive path is formed in the dielectrics between interconnects⁹⁻¹⁵. It becomes more significant when interconnect pitch scales down because of higher electric field intensity inside the dielectrics. LER can accelerate TDDB by reducing the local wire space and enhancing the electrical field intensity at its protrusions¹¹. In this section, an LER-aware TDDB model is built and yield loss by TDDB is studied.

For low-k dielectrics, the probability that TDDB occurs before time t can be calculated by Eq. (8), assuming the time-to-breakdown t_{BD} obeys Weibull distribution^{10, 11}. β is the Weibull slope. η is the characteristic lifetime of the dielectric, which depends on the electrical field intensity E and the dielectric area A .

$$F(t) = 1 - \exp\left[-(t/\eta(E, A))^\beta\right] \quad (8)$$

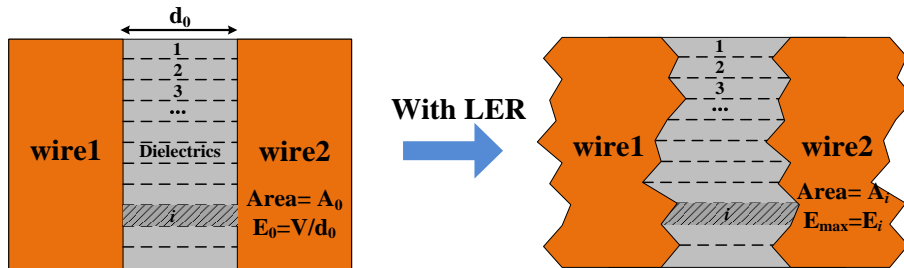


Figure 6. The model for calculating the TDDB failure

Without LER, a uniform electrical field is formed between the signal and ground wire. TDDB can be estimated directly by Eq. (8). However, with LER, the electric field intensity is different along the metal wire due to its geometry variation. Therefore, the dielectrics are divided into segments and the electrical field intensity in the i th segment is E_i , as shown in Figure 6. Then, the TDDB probability of each segment is calculated individually by Eq. (8). The TDDB probability in a metal layer can be estimated by Eq. (9), where it is assumed that the dielectric fails as long as one of the segments breaks down. N is the total number of the dielectric segments in a metal layer that are electrically stressed.

$$F(t) = 1 - \prod_{i=1}^N (1 - F_i(t)) = 1 - \prod_{i=1}^N \exp \left[- (t / \eta_i (E_i, A_i))^\beta \right] \quad (9)$$

The characteristic lifetime η_i of the i th segment is determined by Eq. (10), which combines the impact of the dielectric area and electrical field intensity¹⁰. E_0 and A_0 are the electrical field intensity and the area of the dielectric segment without LER, respectively. E_i and A_i are the electrical field intensity and the area of the i th segment, respectively. In this study, E_i is the maximum electric field intensity in the i th segment. γ is the field acceleration factor.

$$\eta(E_i, A_i) / \eta(E_0, A_0) = (A_0 / A_i)^{1/\beta} \exp(-\gamma(E_i - E_0)) \quad (10)$$

To simplify this calculation, the characteristic lifetime in each segment is simulated with the wire model in Figure 6. Then, the probability density function $f(\eta)$ of the characteristic lifetime is obtained by fitting the simulation results¹⁰. Therefore, the TDDB probability of each segment can be calculated as Eq. (11).

$$F_i(t) = 1 - \int \exp \left[- (t / \eta(E_i, A_i))^\beta \right] \cdot f(\eta) d\eta \quad (11)$$

The 1D metal pattern in Figure 3(a) is used to estimate TDDB induced yield loss. The worst situation is considered, where the electric field is applied between each pair of wires. The material parameters of the low-k dielectrics are $\beta=1.01$ and $\gamma=3.79\text{cm/MV}$, which is measured by experiments¹⁴. The characteristic lifetime η of dielectric in a metal layer with 28nm pitch wire is used as the reference, which is obtained from Eq. (10) by assuming its 5-year TDDB probability to be 0.5%.

The 5-year TDDB loss is plotted in Figure 7, where TDDB loss is increased as $3\sigma_{\text{LER}}$ increases. For 24nm pitch wire, TDDB loss is reduced by about 0.3% when wire space is enlarged to 14nm, which can be explained by the reduced electric field intensity with larger wire space. For 28nm pitch wire, the TDDB loss is also reduced when wire space is enlarged to 16nm.

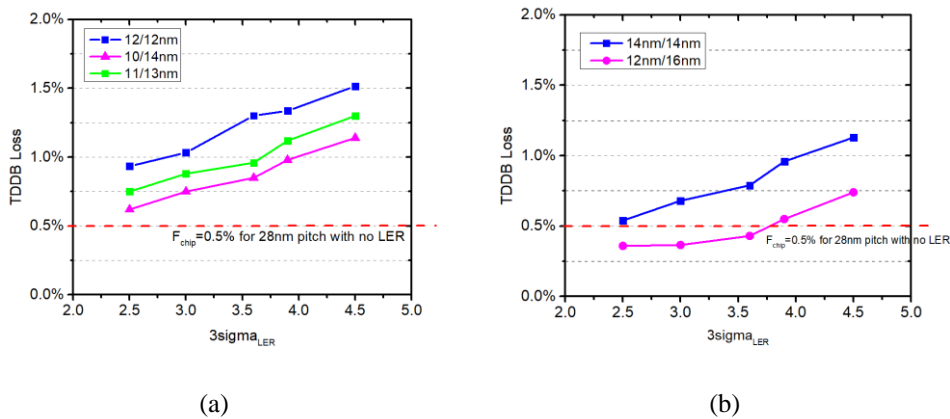


Figure 7 TDDB loss for (a) 24nm pitch wire and (b) 28nm pitch wire

The total yield loss is calculated by combining shorts/opens failure and TDDB. As plotted in Figure 8(a), at $3\sigma_{\text{LER}} = 3.0\text{nm}$, changing the wire geometry from 12nm/12nm to 11nm/13nm can reduce the total yield loss by about 0.2% for 24nm pitch. It can be attributed to the fact that the total yield loss is dominated by TDDB failure while the shorts/opens induced failure is negligible at this $3\sigma_{\text{LER}}$

value. However, when $3\sigma_{\text{LER}}$ rises to a larger value, this method can lead to higher yield loss because of the significant increase of wire opens, as shown in Figure 8(b). This illustrates that the choice of design rule need be carefully co-optimized with LER and TDDB. In this situation, the yield loss can be reduced by increasing the wire pitch. For example, at $3\sigma_{\text{LER}}=3.6\text{nm}$, the yield loss is only 0.55% for 28nm pitch wire with equal space and width while it is 30% for 24nm pitch wire.

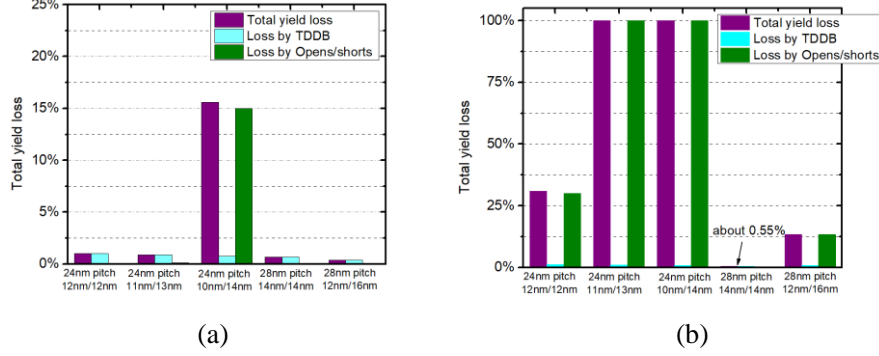


Figure 8 The total yield loss at (a) $3\sigma_{\text{LER}} = 3.0\text{nm}$ and (b) $3\sigma_{\text{LER}} = 3.6\text{nm}$

3. Evaluation of LER impact on Chip Level Metrics

As interconnect pitch scales down to sub-30nm, its performance is becoming more and more important in determining the overall chip performance⁴. However, at smaller wire dimension, the interconnect performance also becomes more vulnerable to process variation, which impacts delay, power consumption and crosstalk in interconnect levels. In this section, the impact of LER on-chip level metrics is evaluated.

A. Critical path delay

Wire geometry variation by LER leads to higher signal delay by increasing wire resistance, since Cu resistivity rises as wire dimension shrinks^{16, 17}. The deviation of signal path delay from its designed value can lead to chip malfunction and adds to yield loss¹⁸. Therefore, critical path delay is modeled and analyzed to evaluate the impact of LER on-chip timing performance.

The critical path delay is modeled by the Elmore's delay model, where an interconnect wire of average length is driven by a chain of inverters¹⁷. The signal delay can be calculated as Eq. (12)¹⁹. R_{drv} and C_{drv} are the output resistance and input capacitance of an inverter, respectively¹⁹. R_w is the wire resistance. C_g and C_c are the ground capacitance and coupling capacitance between wires, respectively, which can be calculated by the model in¹⁸. A size-dependent Cu resistivity model is used to consider the impact of wire geometry variation^{16, 17}. For long wires, buffers are inserted to reduce delay and the delay is calculated as Eq. (13), where the optimal buffer size h and the optimal number of buffers k in the signal path are determined by the Eq. (14)¹⁸. The average wire length L_{avg} is determined by the stochastic wire distribution model based on Rent's rule²¹. The R_w , C_g and C_c are calculated based on L_{avg} .

$$t_{0.5} = k \left[0.7R_{\text{drv}} (C_g + 4.4C_c + C_{\text{drv}}) + R_w (C_g + 1.5C_c + 0.7C_{\text{drv}}) \right] \quad (12)$$

$$t_{0.5} = k \left[0.7 \frac{R_{\text{drv}}}{h} \left(\frac{C_g}{k} + 4.4 \frac{C_c}{k} + hC_{\text{drv}} \right) + \frac{R_w}{k} \left(0.4 \frac{C_g}{k} + 1.5 \frac{C_c}{k} + 0.7hC_{\text{drv}} \right) \right] \quad (13)$$

$$k = \sqrt{\frac{0.4R_w C_g + 1.51R_w C_c}{0.7R_{drv} C_{drv}}}, h = \sqrt{\frac{0.7R_{drv} C_g + 1.4 \times 2.2R_w C_c}{0.7R_w C_{drv}}} \quad (14)$$

In the experiment, wire geometry with LER is generated by conducting inverse Fourier transform from a Gaussian autocorrelation function based power spectral density with random phases⁶. Wires with 24nm pitch (width/space: 12/12nm, 11/13nm and 10/14nm) and 28nm pitch (12/16nm and 14/14nm) are studied, where 5000 geometry samples are tested for each of them. The average length of the wires in M1 is determined by the stochastic wire distribution model based on Rent's rule. 1100 million logic gates are assumed on a 1cm × 1cm chip⁴. Other parameters used are: average fan-out = 3, Rent's coefficient k = 4 and Rent's exponent p = 0.55⁴. The L_{avg} calculated is 0.8μm. A 10μm wire with buffer inserted is also considered.

Figure 9 plots average delay increment with $3\sigma_{LER}=3.0nm$ and 3.6nm, which is normalized by the delay without LER. Larger delay increment is observed for 10μm wires. In Figure 9 (a), for 24nm pitch wires, the average delay increment is increased by 1% when wire space is enlarged to 10nm while it is increased by less than 0.5% for 28nm pitch wires. This result indicates that enlarging wire space to reduce TDDDB has limited impact on wire delay.

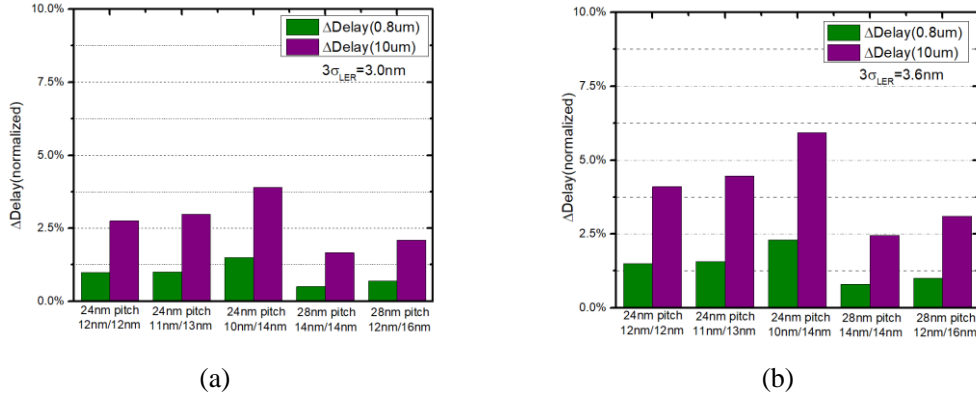


Figure 9 The normalized delay increment at (a). $3\sigma_{LER}=3.0nm$ (b). $3\sigma_{LER}=3.9nm$

B. Chip area penalty

As discussed previously, when LER is high, yield loss is dominated by wire shorts and opens. Wires with larger pitch should be applied to the local metal layer to maintain yield, which induces chip area penalty to maintain chip bandwidth. We estimate the chip area needed to maintain the bandwidth. The bandwidth is estimated based on the delay and the number of wires in each metal layer, as proposed by Gupta *et.al*¹⁹. Chip area is estimated by considering the wiring density in each metal layer, as used by Chi-Shuen Lee *et.al*²². A 7-layer interconnect hierarchy is assumed here²³. The 24nm pitch (or 28nm pitch) wire is applied to M1-M3. The wire pitch is 36nm in M4-M5 and 48nm in M6-M7²³. The estimated chip area is plotted in Figure 10 (a), which is normalized by the chip area with 24nm pitch wire (12nm/12nm). It is observed that about 15% chip area penalty is induced to use 28nm pitch wire in M1-M3.

To consider the chip area penalty, yield is normalized by chip area, as plotted in Figure 10(b). It is observed that when LER is high ($3\sigma_{LER} = 3.6nm$), the metal layer with 28nm pitch wire shows higher yield despite chip area penalty. Therefore, it is concluded that high yield can be maintained when LER is larger at the expenses of additional chip area cost.

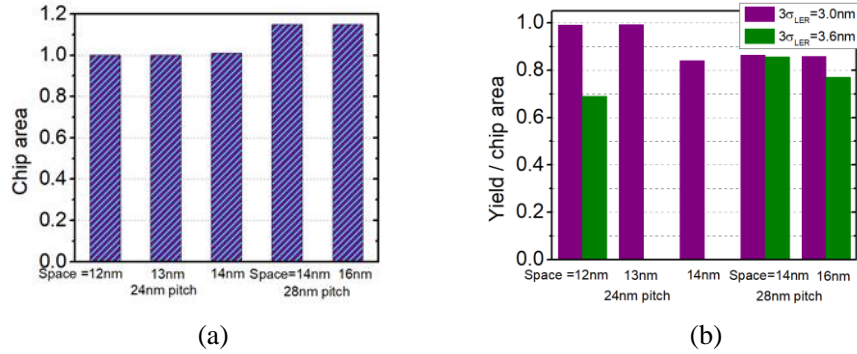


Figure 10 (a). The estimated chip area when using different wire pitch. (b). the ratio between yield and chip area.

IV. Conclusion

In this work, we studied the possibility to pattern sub-30nm Cu metal wires with EUVL under different LER conditions. An analytical and simulation-based yield model is proposed to assess the impact of LER on design yield, which considers LER induced metal wire shorts/opens and enhanced TDDB failure. From the yield analysis, single patterning with EUVL shows higher LER threshold than LELE patterning, which reduces the LER requirement for high yield. Besides, it is observed that when $3\sigma_{LER}$ is small, the total yield loss can be reduced by increasing the wire space, which reduces the TDDB failure. When $3\sigma_{LER}$ is large, yield loss and delay variation are reduced using wires with larger pitch while about 15% chip area penalty is also induced. In our future work, we plan to apply this yield model to estimate the yield of real design work and explore the design rules for LER-aware design.

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