Comprehensive Die-Level Assessment of Design Rules and Layouts

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Introduction

• Impact of new technologies on design is inferred from Design Rules (DRs)

• Process of evaluation of DRs is largely unsystematic and empirical

• Interaction of DRs with layouts, performance, margins, yield requires a fast and systematic evaluation method
Prior Work

UCLA_DRE (ICCAD’09, TCAD’12)

- A framework for early exploration of design rules, patterning technologies, layout methodologies, and library architectures
- Standard cell-level evaluation

Shortcomings

- Not every change in cell area results in a corresponding change in chip area
- Chip area can be affected by buffering and gate sizing to meet timing constraints
Prior Work

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- A framework for early exploration of design rules, patterning technologies, layout methodologies, and library configurations
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**Shortcomings**

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Chip-DRE: Chip level Design Rule Evaluator

- Generates virtual standard-cell library
- Employs semi-empirical and machine-learning-based models

**Good Chips per Wafer (GCPW)**

- unified metric for area, performance, variability and functional yield metrics

\[
\frac{\text{wafer\_area}}{\text{chip\_area}} \times \text{yield}
\]
FLOW OF CHIP-DRE
Chip-DRE Flow

- Design Rule Set
- Cell Usage Statistics
- Library Transistor-Level Netlist

Cell Area Estimator

- Initial cell-area
- Final cell-area

Cell Delay Estimator

- Cell-area scaling factor
- Delay scaling factor

Cell Delay-to-Area Machine Learning Estimation

Cell-Area to Chip-Area Model

Chip Functional Yield Estimator

Good Chips per Wafer

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Chip-DRE Flow

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DRE

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- Initial cell-area
- Final cell-area

Cell-Area to Chip-Area Model

- Chip-area estimate

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Cell Delay-to-Area Machine Learning Estimation

Chip Functional Yield Estimator

Good Chips per Wafer
Chip-DRE Flow

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DRE

Cell Area Estimator

Cell Delay Estimator

Delay scaling factor

Cell Delay-to-Area Machine Learning Estimation
Chip-DRE Flow

- Design Rule Set
- Cell Usage Statistics
- Library Level Transistor-Level Netlist

Cell Area Estimator

- Initial cell-area
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Cell-Area to Chip-Area Model

- Chip-area estimate

Cell Delay Estimator

- Delay scaling factor
- Cell-delay-to-area machine learning estimation

Chip Functional Yield Estimator

- Good chips per wafer

- RC approximation
- Elmore Delay
- Current variability used to estimate worst case delay
Chip-DRE Flow

Design Rule Set → Cell Usage Statistics → Library Transistor-Level Netlist

Cell Area Estimator
- Initial cell-area
- Final cell-area

Cell Area to Chip-Area Model
- Chip-area estimate

Cell Delay Estimator
- Cell-area scaling factor

Cell Delay-to-Area Machine Learning Estimation
- Delay scaling factor

Chip Functional Yield Estimator
- Good Chips per Wafer
Cell Delay-to-Area Model

• Addresses effect of timing optimization during physical synthesis
• Predicts total cell-area scaling factor as cell-delay is scaled
• Based on Machine learning: Neural Network
• Features:
  – number of instances on critical path,
  – average fanout, average interconnect length,
  – average delay and area of gates on critical path,
  – utilization and timing constraint,
  – ratio between area of critical paths to total cell area and
  – delay scaling factor
Cell Delay-to-Area Model

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- Based on Machine learning: Neural Network

![Graphs showing cell area vs. delay scaling factor for MIPS and FPU]
Chip-DRE Flow

- Design Rule Set
- Cell Usage Statistics
- Library Transistor-Level Netlist

1. **Cell Area Estimator**
   - Initial cell-area
   - Final cell area

2. **Cell Delay Estimator**
   - Cell-area scaling factor
   - Delay scaling factor

3. **Cell Delay-to-Area Machine Learning Estimation**

4. **Cell-Area to Chip-Area Model**
   - Chip-area estimate

5. **Chip Functional Yield Estimator**

6. **Good Chips per Wafer**
Cell-area to Chip-area Model

- Semi-empirical model to estimate chip-area in terms of cell-area
- Accounts for routing-limited designs
- Coefficients fitted from P&R experiments
  - Use AEGR (Area estimation using Global Routing)
    - Estimate maximum utilization such that design is routable
    - Up to 7x speedup

\[
\begin{align*}
y &= x + (y_0 - x_0) \times \left( \frac{x_0}{x} \right) \frac{x_0}{y_0 - x_0} \quad \text{for } x > x_0, \\
y &= y_0 \quad \text{for } x \leq x_0.
\end{align*}
\]

\(x\) : total cell-area
\(y\) : chip-area
\(x_0, y_0\) : fitting coefficients
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- Total cell-area
- Chip-area
- \( x_0, y_0 \): fitting coefficients

![Graphs showing the relationship between cell area and chip area for different components.](image)
Chip-DRE Flow

**Using DRE:**
Overlay, contact hole, random particle defects

Using DRE:
Overlay, contact hole, random particle defects

**Cell Delay Estimator**
Delay scaling factor

**Cell Delay-to-Area Machine Learning Estimation**

**Cell-Area to Chip-Area Model**

**Cell-Area Estimator**
Initial cell-area
Final cell-area

**Chip Functional Yield Estimator**
Chip-area estimate

**Good Chips per Wafer**

**Design Rule Set**

**Cell Usage Statistics**

**Library Transistor-Level Netlist**
SAMPLE STUDIES USING CHIP-DRE
Well-to-active Spacing Rule Exploration

- As Well-to-active spacing rule increases:
  - Cell area increases
  - Cell delay decreases due to well proximity effect
- Dependence of GCPW and chip-area on the rule value is non-monotone!
- Verified against PR runs, with max error of 3%
FinFET Fin-Pitch Study

- Fin pitch effect on chip area of FPU
- Fin pitch of 60nm through 100nm, cell area is steeply increasing while chip area is slightly changing
- Error <5%
Local Interconnect-to-poly Spacing Study

• As LI-to-poly space increases
  – Cell area increases
  – Cell delay changes: capacitive coupling decreases but diffusion capacitance may increase

• Study shows cell-area increase dominates over potential chip-area decrease

![Graph showing chip area and GCPW against poly to LI spacing](image-url)
Conclusion

• Introduced Chip-DRE framework for fast and systematic evaluation of design rules and library architectures at chip-scale

Future Work

• Include Power optimization
• Extend to back-end rules and use Chip-DRE to develop DR and library projections for 5nm node
QUESTIONS ?
BACKUP
Cell Delay Estimation
Yield Estimator

- Using **DRE**
- Considers probability of survival from:
  - **Overlay error**: Normal distribution
  - **Random Particle Defects**: Critical area analysis + negative binomial yield model
  - **Contact hole failure**: Poisson distribution
## Numeric Results for WPE Experiment

<table>
<thead>
<tr>
<th>Well-to-active spacing [nm]</th>
<th>Run-time (SPR) [min]</th>
<th>Cell-Area (Chip-DRE) [um²]</th>
<th>Chip-Area (Chip-DRE) [um²]</th>
<th>Error [%]</th>
<th>GCPW (Chip-DRE)</th>
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<tr>
<td>140</td>
<td>118</td>
<td>28171</td>
<td>30364</td>
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<td>207</td>
<td>32554</td>
<td>32787</td>
<td>-2</td>
<td>616</td>
</tr>
</tbody>
</table>
Variability
Variability

• Current variability index:

\[ \Delta \left( \frac{W}{L} \right) = \frac{\sum_{all \text{ gates}} |\Delta \left( \frac{W}{L} \right)_i|}{\left( \frac{W_{tot}}{L} \right)_{ideal}} \]

• Modeling delta W/L for each source of variability from literature (tapering, diffusion and poly rounding, CD variability)
Manufacturability

- Manufacturability Index for evaluating DRs is probability of survival (POS) from three major sources of failure
  - contact-defectivity (a.k.a. contact-hole failure);
  - overlay error (i.e. misalignment between layers) coupled with lithographic line-end shortening (a.k.a. pull-back);
  - random particle defects.
Manufacturability (cont’d)

• Contact hole yield follows poisson yield model: \( Y = Y_0 e^{-\lambda} \)
  Lambda is average # failed contacts=# contacts * failure rate.
• Overlay vector components in x and y directions are described by a normal distribution with zero mean & 3\( \sigma \)
• We compute POS from overlay causing: failure to connect between contact and poly/M1/diffusion, gate-to-contact short defect, and always-on device caused by poly-to-diffusion overlay error
• For failure caused by random particles, critical area analysis for open and short defects at M1/poly/contact layers and short defects between gates and diffusion-contacts.
• \( \text{Yield} = \text{yield}_{\text{contact}} \times \text{yield}_{\text{overlay}} \times \text{yield}_{3\text{ randomParticles}}; \)