Incremental Gate Sizing for Late Process Changes

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Outline

1. Process change
2. ECO Costs
3. ECO Aware Design via LPECO
4. Experiments
5. Summary
Manufacturing process

• The foundry provides designers with a model of the manufacturing process
  – Information about the way transistors and interconnect
  – BSIM / PTM models, Liberty (.lib) model

• Model contains information about:
  – Electrical parameters: threshold voltage, saturation current, leakage current, I-V characteristics, interconnect resistance, capacitance, dielectric information
  – Geometrical parameters: gate length, gate width, source / gate / drain capacitance
Manufacturing Process Changes

- Aggressive schedules = uncertainty
  - From ITRS 2008:

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normalized mask cost from public and IDM data</td>
<td>1</td>
<td>1.3</td>
<td>1.7</td>
<td>2.3</td>
<td>3</td>
<td>3.9</td>
</tr>
<tr>
<td>% $V_{dd}$ variability: % variability seen in on-chip circuits</td>
<td>10%</td>
<td>10%</td>
<td>10%</td>
<td>10%</td>
<td>10%</td>
<td>10%</td>
</tr>
<tr>
<td>% $V_{th}$ variability: doping variability impact on $V_{th}$, (minimum size devices, memory)</td>
<td>31%</td>
<td>35%</td>
<td>40%</td>
<td>40%</td>
<td>40%</td>
<td>58%</td>
</tr>
<tr>
<td>% $V_{th}$ variability: includes all sources</td>
<td>33%</td>
<td>37%</td>
<td>42%</td>
<td>42%</td>
<td>42%</td>
<td>58%</td>
</tr>
<tr>
<td>% $V_{th}$ variability: typical size logic devices, all sources</td>
<td>16%</td>
<td>18%</td>
<td>20%</td>
<td>20%</td>
<td>20%</td>
<td>26%</td>
</tr>
<tr>
<td>% CD variability</td>
<td>12%</td>
<td>12%</td>
<td>12%</td>
<td>12%</td>
<td>12%</td>
<td>12%</td>
</tr>
<tr>
<td>% circuit performance variability, circuit comprising gates and wires</td>
<td>46%</td>
<td>48%</td>
<td>49%</td>
<td>51%</td>
<td>60%</td>
<td>63%</td>
</tr>
<tr>
<td>% circuit total power variability, circuit comprising gates and wires</td>
<td>56%</td>
<td>57%</td>
<td>63%</td>
<td>68%</td>
<td>72%</td>
<td>76%</td>
</tr>
<tr>
<td>% circuit leakage power variability, circuit comprising gates and wires</td>
<td>124%</td>
<td>143%</td>
<td>186%</td>
<td>229%</td>
<td>255%</td>
<td>281%</td>
</tr>
</tbody>
</table>

Solutions known, under development  
Solutions not known
45nm Manufacturing Process change Example

- From April 2008 to March 2010
  - Real data from a commercial 45nm process

![Graph showing NMOS and PMOS parameters comparison]
Engineering Change Order (ECO)

• Design changes that are made late in the design process are referred to as an Engineering Change Order (ECO)

Example:

HotFab Foundry provides Design Tech Inc. with an updated set of manufacturing parameters that decrease $I_{sat}$ (the saturation current), causing their current designs to violate timing.

They fix their design using an ECO which includes changing the gate sizes (e.g. INV X1 -> INV X8), and routing changes

ECO = design / tool time + delays! (€€€ / $$$ !)
ECOs should minimize implementation costs!
What does an ECO cost?

Legend

- Added nets
- Deleted nets
- Moved cells
- Resized cells

Quantify ECO cost → Guide Optimization
Proposed Measures for ECO Cost

• **ECO Area Cost:** Changed area
  – Amount of area that must be reanalyzed for
    • Parasitic Extraction & LVS / DRC
    – Potential layout errors to be corrected

• **ECO Timing Cost:** Changed timing
  – The effect of the ECO on the timing signal (circuit topology):
    • # of pins with unnecessary timing changes
      – The pin was not violating timing before the ECO
    – Changes cause slew, crosstalk violations, in paths that run through the ECO
    – Potential timing errors to be corrected
ECO Area Cost

• Measured as the amount of area, in \( \mu m^2 \) that has changed
  – Includes gate area, metal wires and vias
Estimating ECO Area Cost

• Performing trial ECOs are too costly:
  – Impractical to try all possible ECO moves
  – Estimates of routing cost are needed to guide optimization

• Area Cost Estimated as a linear function of:
  – Number of changed pins
  – Number dislocated pins
    • Old and new locations do not overlap
  – Area of the pin bounding box
  – Congestion over the pin bounding box
Estimating ECO Area Cost

• Area Cost Estimate:

\( m_1 \): Number of affected pins
\( m_2 \): Number of dislocated pins (old locations and new locations do not overlap)
\( m_3 \): Pin bounding box area
\( m_4 \): Utilized area over pin bounding box (routing over all layers)

\[
\hat{C}_{\text{area}} = \sum_{i=1}^{4} a_i m_i + b
\]

\( a_1 = 0.0367 \, \mu m^2/\text{pin} \)
\( a_2 = 0.186 \, \mu m^2/\text{pin} \)
\( a_3 = 5.35 \)
\( a_4 = 9.65 \)
\( b = 0.264 \, \mu m^2 \)
ECO Timing Cost

• Timing is affected downstream and upstream
• ECO Timing cost is defined as:
  – # of non-critical pins that are upstream and downstream from an ECO

\[ \text{ECO Timing Cost} = \text{\# of non-critical pins upstream and downstream} \]
ECO Cost Example:

**Timing cost:**
118.9 µm²

**Pin Cost:**
2838 pins
ECO Cost Example:

Timing cost:
586.6 µm²

Pin Cost:
10198 pins
**ECO-cost aware design via LPECO**

- Linear programming based ECO gate sizing
  - Objective: ECO cost + Power cost
  - Constraints: Delay (timing closure)
  - Timing, power and ECO are modeled as a function of the candidate gate size

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**Example: Gate 1**

**Gate Size Candidates**

<table>
<thead>
<tr>
<th>X1</th>
<th>X4</th>
<th>X8</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

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**Current size**

- X2
  - Timing cost: 1
  - Area cost: 2
  - Power cost: 1
  - Delay: 4

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**ECO-cost aware design via LPECO**

minimize \[ \sum_{i,k} p_{ik} y_{ik} + \gamma_t \hat{c}_{\text{timing}} (y; x) + \gamma_a \hat{c}_{\text{area}} (y; x) \]

subject to \[ t_i + d_{i0} + \sum_k \delta_{ik} y_{ik} \leq t_j, \quad \forall i \in \text{fo}(j) \]

\[ t_i \leq T_{\max} \]

\[ \sum_k y_{ik} \leq 1, \quad \forall i \]

\[ 0 \leq y_{ik} \leq 1 \]

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**Example: Gate 1**

<table>
<thead>
<tr>
<th>Gate Size Candidates</th>
<th>X1 ((y_{11} = 1))</th>
<th>X4 ((y_{14} = 1))</th>
<th>X8 ((y_{18} = 1))</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Current size</strong></td>
<td>X2</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Timing cost:</strong></td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td><strong>Area cost:</strong></td>
<td>2</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td><strong>Power cost:</strong></td>
<td>(-1 (p_{11}))</td>
<td>(3 (p_{11}))</td>
<td>(7 (p_{11}))</td>
</tr>
<tr>
<td><strong>Delay change:</strong></td>
<td>(4 (\delta_{11}))</td>
<td>(3 (\delta_{14}))</td>
<td>(2 (\delta_{18}))</td>
</tr>
</tbody>
</table>

\( t \): arrival time for gate \( i \)
\( d_{i0} \): current delay for gate \( i \)
\( \delta_{ik} \): change in delay of gate \( i \) under size \( k \)
\( y_{ik} \): assignment variable of gate \( i \) to size \( k \)
\( p_{ik} \): change in leakage power of gate \( i \) to size \( k \)

(\( \delta_{ik}, d_{i0} \) are from the commercial tool)
Experimental Setup

- 45nm Nangate Open Cell Library
- Manufacturing process change:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Nmos</th>
<th>Pmos</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{th}$</td>
<td>-10%</td>
<td>-5%</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>+5%</td>
<td>-5%</td>
</tr>
<tr>
<td>$C_{gate}$</td>
<td>+10%</td>
<td>+10%</td>
</tr>
<tr>
<td>$l_{eff}$</td>
<td>+5%</td>
<td>+5%</td>
</tr>
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- ECO’s are performed by a leading commercial design tool
- Runtime of LPECO ~.01 to 103s
Experimental Setup

<table>
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<th></th>
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Synthesized Netlist → Commercial Design Tool → Placed and Routed Design

Incremental Optimization (Commercial Design Tool) → Commercial ECO

(Number Manufacturing Process)

Generate Timing Data (Arrival Times and Slacks) → Timing Feasible?

ECO Cost Model → LP → ECO Instructions

ECO Instructions → Commercial Design Tool → LPECO
Results: Area Cost Comparison

Normalized Area Cost

90% Utilization
alu
c7552
c6288
c5315
c3540
c2670
c1908
c1355

80% Utilization
alu
c7552
c6288
c5315
c3540
c2670
c1908
c1355

LPECO
Commercial
Results: Timing Cost Comparison

- 90% Utilization
  - LPECO vs. Commercial
  - Identification of alu, c7552, c6288, c5315, c3540, c2670, c1908, c1355

- 80% Utilization
  - Similar comparison as 90% Utilization
  - Additional identification of alu, c7552, c6288, c5315, c3540, c2670, c1908, c1355

Normalized Timing Cost

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Results: Leakage Power

Normalized Leakage Power

90% Utilization

c7552
alu
c1355

80% Utilization

alu

LPECO
Commercial

John Lee (lee@ee.ucla.edu)
Results: Slack (Infeasible Cases)

Normalized Slack (ns)

-1.600 -1.400 -1.200 -1.000 -0.800 -0.600 -0.400 -0.200 0.000

alu
c7552
c6288
c5315
c3540
c2670
c1908
c1355

LPECO
Encounter

(LP based timing closure)
Summary

• Quantified ECO Costs:
  – ECO Timing Cost
  – ECO Area Cost

• Performed incremental optimization to minimize ECO costs using LPECO

• Method performs well compared to commercial tool:
  – 22% to 88% reduction in ECO Area
  – 1% to 67% reduction in ECO Timing Cost

• Future goals:
  – Initial designs that incur small ECO penalties in the future
  – Large scale examples