Measurement and Optimization of Electrical Process Window

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Outline

• Definition and evaluation of
  – Geometric Process Window (GPW)
  – Electrical Process Window (EPW)
• EPW vs GPW
• Improving EPW
• EPW Approximations
Process Window

- Definition of process window:
  - The range of process parameters that allows circuits to operate under desired specifications [1].

Geometric Process Window (GPW)

- Process parameters are within GPW iff $|\text{critical dimension (CD)}| < \text{allowed CD deviation}$
- Edge placement error (EPE)

2 scenarios are considered:

1. $\text{CD} = L_{\text{nom}} \pm 2\times \text{maximum EPE (W-GPW)}$
2. $\text{CD} = L_{\text{nom}} \pm \text{maximum EPE (A-GPW)}$
Problems of GPW

1. Geometric tolerance does not quantify changes in electrical specifications well.
   - Averaging across transistor segments
     - A transistor segment may violate geometric tolerance but the transistor can work within desired electrical specification
   - Averaging across multiple transistors
     - $\Delta$Delay averages across critical path
     - $\Delta$Power averages across all transistors

2. Not all shapes are critical but equal effort/resources are dedicated.
Electrical Process Window

• A process point is considered within EPW iff

\[
\text{Lower bound of allowed circuit performance} \leq \text{Circuit performance} \leq \text{Upper bound of allowed circuit performance}
\]

• Need to extract circuit performance of printed contours
  – Modeling non-rectangular gate transistor
• Impact of interconnect linewidth variation is relatively smaller compared to the impact of gate length variation on transistor [2]
  – Width variation averages over long wires.
  – Resistance and capacitance change in opposite directions as line width changes.

Modeling non-rectangular transistor [3]

- Slice simulated transistor channel
- Calculate $V_{th}$, effective width and length of each slice
- Find the total $I_{on}$ and $I_{off}$

Delay centric EPW (DEPW)

• A process point is considered within DEPW iff
  \[ \text{Max}(\Delta \text{ path delay}) \leq \text{Upper bound of allowed delay deviation} \]

• Assume cell delay is inversely proportional to \( I_{\text{on}} \)

\[
\text{Cell delay} = \frac{\sum_{j=1}^{N_i} I_{\text{on-original-j}}}{\sum_{j=1}^{N_i} I_{\text{on-simulated-j}}} \times \text{original cell delay}
\]

- Extract \( I_{\text{on}} \) from simulated contour and original layout
- Obtained from timing report

• Path delay is the sum of delay of each cell

\[
D_{\text{path-simulated}} = \sum_{i=1}^{M} (\text{Cell delay}_i)
\]
Leakage Power Centric EPW (PEPW)

- A process point is considered within PEPW iff
  \[ \Delta \text{power} \leq \text{Upper bound of allowed leakage power deviation} \]

- Leakage power is proportional to \( I_{\text{off}} \)

\[
\Delta \text{power} = \left[ \frac{\sum_{j=1}^{T} I_{\text{off\_simulated\_j}}}{\sum_{j=1}^{T} I_{\text{off\_original\_j}}} - 1 \right] \times 100\%
\]

Extract \( I_{\text{off}} \) from simulated contour and original layout.
Combined EPW (CEPW)

- Process window of multiple electrical metrics: Intersection of EPWs

\[ \text{CEPW} = \bigcap_{i=1}^{Q} (\text{EPW}_i) \]
Relation between EPW and GPW

- GPW and EPW are defined differently
  - Need to know relation between them for fair comparison
- Simulate an INV (FO4) at worst case corners of W-GPW using SPICE, measure the delay and power deviation

<table>
<thead>
<tr>
<th>Δ Channel length (%)</th>
<th>W-GPW Δ EPE (%)</th>
<th>A-GPW Δ EPE (%)</th>
<th>DEPW Δ delay (%)</th>
<th>PEPW Δ power (%)</th>
</tr>
</thead>
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<tr>
<td>5</td>
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<td>5</td>
<td>11</td>
<td>54</td>
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<td>10</td>
<td>5</td>
<td>10</td>
<td>21</td>
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<td>15</td>
<td>7.5</td>
<td>15</td>
<td>30</td>
<td>2476</td>
</tr>
</tbody>
</table>

Use SPICE model and layout from 45nm Nangate Open Cell library (Vdd = 1.1V, Temperature = 25°C)
Analysis Flow

Design: ISCAS-85 benchmark circuits

45nm Nangate Open Cell Library

Synthesis, place and route

Layout (original), timing report

Layout after OPC

Run OPC at nominal process point

Simulate layout using different process parameters

Exposure (%) ∈ {80, 90, 100, 110, 120}
Defocus (nm) ∈ {0, 40, 80, 160}

Simulated contours

△ Delay & △ Power Extraction

EPW Extraction

GPW Extraction

Filter printed contour with short or open circuit
GPW vs EPW

• GPW is pessimistic because
  1. GPW: Limit by worst transistor segment deviation
     EPW: Average deviation of each transistor segment
  2. Averaging across multiple transistors
     • $\Delta$Delay averages across critical path
     • $\Delta$Power averages across all transistors
  3. All transistors are not equally important
     $\Rightarrow$ Delay constraint is applied on critical path only

• EPW is 1.5 to 6X larger than AGPW on average
Improving EPWs

• Layout transparent process tuning
  – Avoid major change in layout
• Increasing $V_{th}$ or gate length

• We tried:
  ▪ -2nm on critical cells
  ▪ +2nm on non-critical cells
  ▪ +/-2nm on all cells (i.e., a global CD push)
  ▪ +/-20mV on all cells (i.e., a global $V_{th}$ push)
Improved DEPW and PEPW

Area of improved DEPWs normalized to reference DEPW

Area of improved PEPWs normalized to reference PEPW
Improved CEPW

- Reducing $V_{th}$ on all cells
  - Improves CEPW consistently
  - Can be done without knowing the locations of critical cells
  - -2nm gate length bias does not work as well due to increased pinching
EPW Approximation

Motivation: Critical path of a design may not be provided to lithography process

Method 1: Use EPE histogram generated in OPC
- Estimate EPW without extracting channel shape of each transistor
- Approximate average delay and power deviation induced by EPEs of all transistors as an equivalent transistor

\[
\text{histogram-DEPW} \iff \left[ \frac{I_{on-reference-transistor}}{I_{on-equivalent-transistor}} - 1 \right] \times 100\% \leq \text{upper bound of allowed delay deviation}
\]

\[
\text{histogram-PEPW} \iff \left[ \frac{I_{off-equivalent-transistor}}{I_{off-reference-transistor}} - 1 \right] \times 100\% \leq \text{upper bound of allowed power deviation}
\]
Method 2 : Use the shape of every transistor

- \( I_{\text{off}} \) of each transistor is available => No approximation on PEPW
- Delay deviation of each transistor:
  \[
  \Delta \text{Delay} = \left[ \frac{I_{\text{on-original}}}{I_{\text{on-simulated}}} - 1 \right] \times 100\%
  \]
- A process point is considered within DEPW iff
  \[
  \frac{\sum_{n=1}^{R} \Delta Delay_n}{R} \leq \text{upper bound of allowed delay deviation}
  \]
  Average delay deviation of \( R \) transistors with worst delay deviation
- \( R = 1 \), Lower bound of DEPW but too pessimistic
- \( R = 30 \), Critical path is usually more than one transistor
  => Average transistor stages along critical path
- \( R = \) Total transistors, Assume EPE distribution on critical path is similar to that of all transistor
Approximation quality

Reference DEPW only consider transistor along critical path but approximate DEPW uses histogram of entire design (more averaging)

- All approximations have better area coverage compared to A-GPW
- Low area coverage in histogram-PEPW leads to poor coverage in histogram-CEPW
- Approximation using the shape of each transistor is the best:
  - No area out of EPW, covered 80% area of reference EPW
Summary

• We propose EPW which is a better measure of process window than conventional GPW
• Area of EPW is 1.5 to 6 times larger than that of GPW on average
• Layout transparent methods can improve EPW by 10%
• Approximation to EPW covers 80% of the area of reference EPW for all benchmark circuits
• Future work: Analyzing only representative layouts
  – Reduce lithography simulation runtime in EPW calculation
  – Can be used for OPC recipe optimization
Backup slides
Results: EPW Approximations

DEPW
\(\Delta\) Delay \(\leq 21\%\)

PEPW
\(\Delta\) Power \(\leq 311\%\)

CEPW
\(\Delta\) Power \(\leq 311\%\)
\(\Delta\) Delay \(\leq 21\%\)