On Electrical Modeling of Imperfect Diffusion Patterning

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Outline

• Motivation
• Modeling Diffusion Rounding
• Parameter Extraction
• Experimental Results
• Conclusions
Lithographic WYSIWYG Breakdown

• Existing compact device models (e.g., BSIM) do not handle non-rectangular geometries.

• Sources of diffusion rounding:
  – Different channel widths with tight poly pitch
  – Power/Ground diffusion straps

• Large poly-active corner spacing is required to avoid diffusion rounding → area overhead

Figure from V. Moroz, M. Choi, & X.W. Lin, SPIE 2009.
Previous Works

• Modeled polysilicon rounding/line edge roughness only [SPIE’06, DAC’07, etc]
  – Assumed current flows in horizontal direction
  – Modeled non-rectangular gate device by slicing device’s channel and connecting them in parallel

• Empirical diffusion rounding model [ASPDAC’08]
  – Fitted $I_{on}$ and $I_{off}$ functions based on available data
  – Did not model asymmetrical currents for drain/source side rounding
This Work

• *First* Poly + diffusion rounding model.
  – Developed ground up from fundamental physics

• Models asymmetrical currents for drain/source side rounding.

• SPICE-based calibration of the model
  – No need for silicon or TCAD simulation data.
Modeling Diffusion+Poly Rounding

Slice channel

Extract parameters:
• Channel width
• Channel length
• $V_{\text{th}}$

Obtain total current using SPICE simulation

Equivalent $W, L, V_{\text{th}}$

Channel width deviation

Location dependent channel length

Drain

Source
Channel Slicing

- Channel’s electrostatic potential is two-dimensional
  - Changes $L_{\text{eff}}$ and $W_{\text{eff}}$

- Strategy: divide channel into 3 sections.

- Assume E field is:
  - Purely horizontal in middle.
  - Changing linearly from middle to edges.

**Electrostatic potential**

**TCAD simulation**
Slicing Guideline: ‘S’

- $a, b$ and $L_{\text{eff-ref}}$ are technology independent parameters extracted from TCAD data.
  
  \[ S = \frac{(a + b\theta) \times L_{\text{eff}}}{L_{\text{eff-ref}}} \]

  \[ a = 8\text{nm}, b = 0.089\text{nm}^{-1} \text{ and } L_{\text{eff-ref}} = 25\text{nm} \]

- $\theta$ and $L_{\text{eff}}$ are geometrical parameters extracted from device’s shape.

- Larger $\theta$ (larger source/drain widths) leads to stronger vertical (z) E-field and a larger $S$.

- But increased source/drain is further away from channel → vertical E-field and $S$ weakly dependent on $\theta$.

- Horizontal (y) field changes linearly with channel length → modeled as a multiplier, $L_{\text{eff}}/L_{\text{eff-ref}}$. 
Effective Channel Length

- Middle section of device’s channel is sliced into small transistors with equal source and drain widths
- Source and drain of edge sections are divided into slices equally
  - Assume E-field/current follows the direction of slices
  - Effective channel length of each slice, $L_{\text{eff-i}} = L_i$
Effective Channel Width

• Effective width of sliced channel

\[ W_{eff} = \frac{(W_s - W_d)}{\ln(W_s/W_d)} \]

\( W_{d_i} \) and \( W_{s_i} \) are obtained by approximating edges with straight lines orthogonal to the vector of channel length.

• \( W_{eff} \) is derived based on gradual channel approximation → voltage varies gradually from drain to source

\[ \int_0^L \left( W_d + (W_s - W_d)\frac{y}{L} \right) I_D \, dy = \int_{V_s}^{V_d} \mu C_{ox} [V_G - V_{th} - V] \, dV \]

\[ I_D = \frac{1}{L \ln(W_s/W_d)} \frac{(W_s - W_d)}{\mu C_{ox}} [V_G - V_{th} - \frac{V_{ds}}{2}] \, V_{ds} \]

• Channel width varies along channel

• Second order effects (DIBL, velocity saturation, etc.)
  • Considered by applying effective length, width and \( V_{th} \) in SPICE simulation with BSIM model.
\(\Delta V_{th} - \text{Narrow Width Effect (NWE)}\)

\[\Delta V_{th\text{-effective}} = \Delta V_{th\text{-Narrow width}} + \Delta V_{th\text{-CS}}\]

- Non-uniform \(V_{th}\) along channel width
  - Impact of NWE is modeled by fitting \(\Delta V_{th}\) as a function of location [SPIE’06]

\[
\Delta V_{th}(x) = \begin{cases} 
K_1(x-w)^2 + K_2(x-w) & 0 \leq x \leq w \\
0 & w \leq x \leq W-w \\
K_1(W-x-w)^2 + K_2(W-x-w) & W-w \leq x \leq W 
\end{cases}
\]

- \(w\) is the maximum width affected by NWE
- \(W\) is device's average width
- \(K_1 = 1.65\ (\text{NMOS})\ 0.01\ (\text{PMOS})\)
- \(K_2 = 1.65\ (\text{NMOS})\ 0.01\ (\text{PMOS})\)
- \(w = 5\text{nm}\ (\text{NMOS})\ 1\text{nm}\ (\text{PMOS})\)

Fitted based on rectangular devices data
**ΔV_{th} – Asymmetrical Source/Drain**

- A portion of depletion region is shared between gate and source/drain
- Asymmetric source/drain sharing regions change effective region supported by gate alone \( \rightarrow V_{th} \) variation
- Charge Sharing Model:
  - \( \Delta V_{th} \propto Q_{\text{shared}} \)
  - Estimate \( Q_{\text{shared}} \) based on device’s geometry

\[
V_{th} = V_{fb} + 2\phi_b + \left[ \frac{Q_{\text{total}} - Q_{\text{shared}}}{C_{ox}WL} \right]
\]

\[
Q_{\text{shared}} = qN_a \left( \frac{W_c}{2} \right)(L_dW_d + L_sW_s)
\]

\[
\Delta V_{th-CS} = \frac{qN_aW_c}{2LC_{ox}} \left[ \frac{2(L_dW_d + L_sW_s)}{W_d + W_s} - (L_d + L_s) \right]
\]
Total Currents

• Each slice can be represented by rectangular transistor with equivalent L, W and $V_{th}$:

$$I_{total} = \sum_{i=1}^{n} f(L_i, W_i, V_{th_i})$$

• Second order effects are implicitly considered in BSIM.

• Evaluate $I_{total}$ at $V_{gs} = 0$, $V_{ds} = V_{dd}$ (off)
  $$V_{gs} = V_{dd}, V_{ds} = V_{dd}$$ (on)

Can be obtained using conventional compact model e.g., (BSIM).
Equivalent Rectangular Transistor for Circuit Simulation

Total $I_{on} / I_{off}$

Fit $W_{eff}$ and $L_{eff}$ of a rectangular device to match $I_{on} / I_{off}$

Rectangular device which can be used in SPICE.
Parameter Extraction

- Channel length and width
  - Obtained directly from shapes.
- $\Delta V_{th} = \Delta V_{th-narrow\ width} + \Delta V_{th-cs}$

$$\Delta V_{th-CS} = \frac{q N_a W_c}{2 LC_{ox}} \left[ \frac{2(L_d W_d + L_s W_s)}{W_d + W_s} - (L_d + L_s) \right]$$

Unkowns: charge sharing regions contributed by source and drain.

- $L_d$ and $L_s$ can be calibrated using
  - Silicon data or TCAD simulation results
  - SPICE (+ BSIM) simulation results
TCAD-Based Calibration

- Require $I_{\text{off}}$ of a diffusion rounded device (forward and reverse bias)
- $L_d$ and $L_s$ are calibrated to minimize error between model and measured $I_{\text{off}}$
- $I_{\text{off}}$ is used for calibration as it is sensitive to $V_{\text{th}}$ variation caused by $L_d$ and $L_s$
  
  $L_d = 5 \text{ nm (NMOS)}$  $5.5 \text{ nm (PMOS)}$
  $L_s = 1 \text{ nm (NMOS)}$  $1.0 \text{ nm (PMOS)}$
SPICE Based Parameter Extraction

- Extract $L_d$ and $L_s$ from rectangular devices.
- Perturb $L$ and $V_{ds}$ to obtain $\Delta V_{th}$,
  \[
  K_1 = V_{th,L1} - V_{th,L2}
  \]
  \[
  K_2 = V_{th} \big|_{V_{ds}=V_{dd}} - V_{th} \big|_{V_{ds}=0}
  \]
  Eq. 1
  Eq. 2

Let

\[
\frac{qN_a W_c}{C_{ox}} (L_d) = K_1 \left( \frac{L_1 L_2}{L_1 - L_2} \right) - \frac{K_2 L_1}{2}
\]

\[
\frac{qN_a W_c}{C_{ox}} (L_s) = K_1 \left( \frac{L_1 L_2}{L_1 - L_2} \right) + \frac{K_2 L_1}{2}
\]

Combine Eq. 1 and Eq. 2

$L_d$ and $L_s$ are not fully extracted but they can be substituted into $\Delta V_{th}$ equation directly.

- Extract parameters at large length and width to decouple second order effects
- Less accurate compared to TCAD based calibration as $L_d$ and $L_s$ are not extracted → cannot evaluate source/drain widths in charge sharing region → approximate them as source/drain widths at junctions.
## Simulation Setup

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drawn gate length</td>
<td>45 nm</td>
</tr>
<tr>
<td>Effective channel length</td>
<td>25 nm</td>
</tr>
<tr>
<td>Width (NMOS/PMOS)</td>
<td>110-300 / 255-500 nm</td>
</tr>
<tr>
<td>Vdd</td>
<td>1 V</td>
</tr>
<tr>
<td>Tox</td>
<td>1.5 nm</td>
</tr>
<tr>
<td>S/D doping (NMOS/PMOS)</td>
<td>3e20 / 2e20 cm⁻³</td>
</tr>
<tr>
<td>NSUB (NMOS/PMOS)</td>
<td>2.5e18 / 2.5e18 cm⁻³</td>
</tr>
<tr>
<td>Junction depth</td>
<td>20 nm</td>
</tr>
<tr>
<td>Line-end extension</td>
<td>20 nm</td>
</tr>
<tr>
<td>Spacer width</td>
<td>30 nm</td>
</tr>
</tbody>
</table>

TCAD : Sentaurus 3D
Experiment Flow (SPICE calibrated)

- Geometrical parameters
- Calibrated $\beta L_d$ and $\beta L_s$
- Rectangular devices simulation data (TCAD)
- BSIM model
- Extract $L_{eff}$, $W_{eff}$, and $V_{th}$
- Obtain total current using SPICE simulation
- Diffusion + Poly rounded simulation data (TCAD)
TCAD vs Model (Diffusion Rounding only)

- Asymmetrical $I_{\text{on}}/I_{\text{off}}$ when rounding happens on Drain/Source terminals
  - $\Delta V_{\text{th}}$ varies according to drain/source ratio.
## Poly+Diffusion Rounding

<table>
<thead>
<tr>
<th></th>
<th>( L_1 ) (nm)</th>
<th>( L_2 ) (nm)</th>
<th>( W_d ) (nm)</th>
<th>( W_1 ) (nm)</th>
<th>( W_2 ) (nm)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TCAD cal.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( I_{on} )</td>
</tr>
<tr>
<td>Diffusion rounding</td>
<td>45</td>
<td>45</td>
<td>155</td>
<td>26</td>
<td>0</td>
<td>-2.1</td>
</tr>
<tr>
<td>only</td>
<td>45</td>
<td>45</td>
<td>155</td>
<td>45</td>
<td>0</td>
<td>-2.0</td>
</tr>
<tr>
<td>(Source side larger)</td>
<td>45</td>
<td>45</td>
<td>155</td>
<td>78</td>
<td>0</td>
<td>-2.8</td>
</tr>
<tr>
<td>Poly rounding only</td>
<td>55</td>
<td>45</td>
<td>155</td>
<td>0</td>
<td>0</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td>35</td>
<td>45</td>
<td>155</td>
<td>0</td>
<td>0</td>
<td>NA</td>
</tr>
<tr>
<td>Poly+ diffusion</td>
<td>55</td>
<td>45</td>
<td>155</td>
<td>45</td>
<td>0</td>
<td>NA</td>
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<tr>
<td>rounding</td>
<td>55</td>
<td>45</td>
<td>155</td>
<td>0</td>
<td>45</td>
<td>NA</td>
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<tr>
<td></td>
<td>35</td>
<td>45</td>
<td>155</td>
<td>45</td>
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<td>NA</td>
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<tr>
<td></td>
<td>35</td>
<td>45</td>
<td>155</td>
<td>0</td>
<td>45</td>
<td>NA</td>
</tr>
</tbody>
</table>

Average error:
- (Diffusion layer rounding only)
  - TCAD calibrated model = 1.6%
  - SPICE calibrated model = 2.7%
- (Poly+ Diffusion layers rounding)
  - SPICE calibrated model = 1.7%
Diffusion Rounding on SRAM

<table>
<thead>
<tr>
<th>Defocus (nm)</th>
<th>Contact/Poly Spacing (nm)</th>
<th>Overlay (nm)</th>
<th>SNM (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>40</td>
<td>0</td>
<td>378.20</td>
</tr>
<tr>
<td>0</td>
<td>20</td>
<td>0</td>
<td>379.30</td>
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<tr>
<td>100</td>
<td>40</td>
<td>0</td>
<td>376.50</td>
</tr>
<tr>
<td>100</td>
<td>20</td>
<td>0</td>
<td>378.70</td>
</tr>
<tr>
<td>0</td>
<td>40</td>
<td>20</td>
<td>377.10</td>
</tr>
</tbody>
</table>

SNM for rectangular device = 378.40 mV

- Diffusion rounding is not significant on SRAM.
  - Second order effects are ignored (AS, PS, AD and PD)
  - Symmetrical layout suppresses SNM variation.

- Results may vary for different optical model and device.
Application on Logic Cells

<table>
<thead>
<tr>
<th></th>
<th>NAND_X1</th>
<th>NOR_X1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Original</td>
<td>Spacing Reduced</td>
</tr>
<tr>
<td>Delay</td>
<td>nominal (no defocus)</td>
<td>1.00</td>
</tr>
<tr>
<td></td>
<td>worst (100nm defocus)</td>
<td>1.05</td>
</tr>
<tr>
<td>Leakage</td>
<td>nominal (no defocus)</td>
<td>1.00</td>
</tr>
<tr>
<td></td>
<td>worst (100nm defocus)</td>
<td>0.91</td>
</tr>
<tr>
<td>area</td>
<td></td>
<td>1.00</td>
</tr>
</tbody>
</table>

- At 100nm defocus
  - Δ Delay = 5%
  - Δ Leakage = 9%
- Design rule can be optimized.

NAND2_X1     NOR2_X1
Sources of inaccuracies

1. Source/drain widths of charge sharing regions vary according to $L_d$ and $L_s$. Exact $L_d$ and $L_s$ are not decoupled in SPICE-based calibration.

2. Drain side width changes when device is under saturation.

3. Piece wise modeling error in channel’s electric field distribution.

Future work

- Captures channel width variation in saturation by estimating channel length modulation.

- Extract capacitance related parameters:
  - Diffusion area and perimeter ($AD$, $PD$, $AS$ & $PS$ in BSIM).
Conclusions

• Diffusion rounding affects channel length, width and $V_{\text{th}}$.
• Modeling error for poly+diffusion rounding are 2.3% ($I_{\text{on}}$) and 1.0% ($I_{\text{off}}$)
• Model can be calibrated using SPICE.
• Applications:
  – Post-lithography circuit analysis.
  – Design rules exploration.