Intro to Random Yield Modeling

Rani S. Ghaida
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Sources of Yield Loss

Yield

Parametric
- Timing
- Speed/Power
- Reliability/Signal Integrity

Functional
- Material
- Systematic
- Random

Y = \frac{\text{Avg # of good dies per wafer}}{\text{Total # of dies per wafer}}

>99%

≈90%

≈85%*

* By ITRS for MPU

This talk
Spot Defects – Shorts

- Conductive defects that create a short-circuit failure

Original layout

Particle defect

Short defect
Spot Defects – Opens

- Non-conductive defects that create an open-circuit failure
Photos of Spot Defects

Open defect

Short defect
Hard vs. Soft Defects

- Soft defect does not affect functionality but may lead to system failure during burn-in or operation.
Yield Modeling – Poisson

• Yield from random defects for all layers

\[ Y = \prod_{l=1}^{L} Y_l \]

• Poisson model for 1 layer (uniformly dist defects)

\[ Y_{Poisson_l} = \prod_{j=1}^{k} e^{-\lambda} = \prod_{j=1}^{k} e^{-D_0 A_c, j} \]

\[ \lambda = \text{Avg # of defects} \]
\[ D_0 = \text{Avg defect density} \]
\[ A_c = \text{Avg critical area} \]
Yield Modeling – Negative Binomial

• Negative Binomial model for 1 layer (gamma dist of defect density)

\[ Y_{NB,l} = \prod_{j=1}^{k} \left(1 + \frac{\lambda}{\alpha}\right)^{-\alpha} = \prod_{j=1}^{k} \left(1 + \frac{A_{c,j}D_0}{\alpha}\right)^{-\alpha} \]

\[ \alpha = \text{Clustering param} \approx 2 \ (ITRS) \]
Critical Area

• Layout area where a defect would cause functional failure
Critical Area

\[ A_{c,j} = \int_0^\infty A_{c,j}(r) \times f_s(r) \cdot dr \]

\( A_{c,j}(r) \) = critical area of defect size \( r \) and type \( j \)

\( f_s(r) \) = defect size distribution

\[ f_s(r) = \begin{cases} 
\frac{2(n-1)r}{(n+1)r_0^2} & 0 \leq r \leq r_0 \\
\frac{2(n-1)r_0^{n-1}}{(n+1)r^n} & r_0 \leq r 
\end{cases} \]

\( n = 3 \)
\( r_0 = 34 \text{nm} \)

Source: ITRS
Critical Area Analysis

• Runtime/Accuracy tradeoff

• Monte Carlo Simulation
  – randomly placing a large number of virtual defects on the layout and checking for device failure for each defect

  \[ A_c(r) = A \times POF = A \times \frac{\text{# of defects causing failure}}{\text{Total # of generated defects}} \]

• Grid Method:
  – critical area is approximated by using a grid over the layout and determining, at every point of the grid, the radius of the smallest defect that causes a failure
Critical Area Analysis – Geometric Method

• Apply a shape-contraction on the layout followed by a shape-expansion and then subtract resulting layout from the original one
Critical Area Analysis

- Virtual artwork approach
  - computing the critical area of a histogram representation of interconnect widths, spacings, and lengths.

- Stochastic Method
  - estimate critical area from statistical features of the layout using analytical model.

\[
S_{\text{open}} = 1 - (1 - d) \frac{(r - w)}{(w + s)}
\]

\[
S_{\text{short}} = 1 - \left[ 1 + \left( \frac{r - s}{w + s} \right) \cdot d \right] \cdot (1 - d) \frac{(r - s)}{(w + s)}
\]