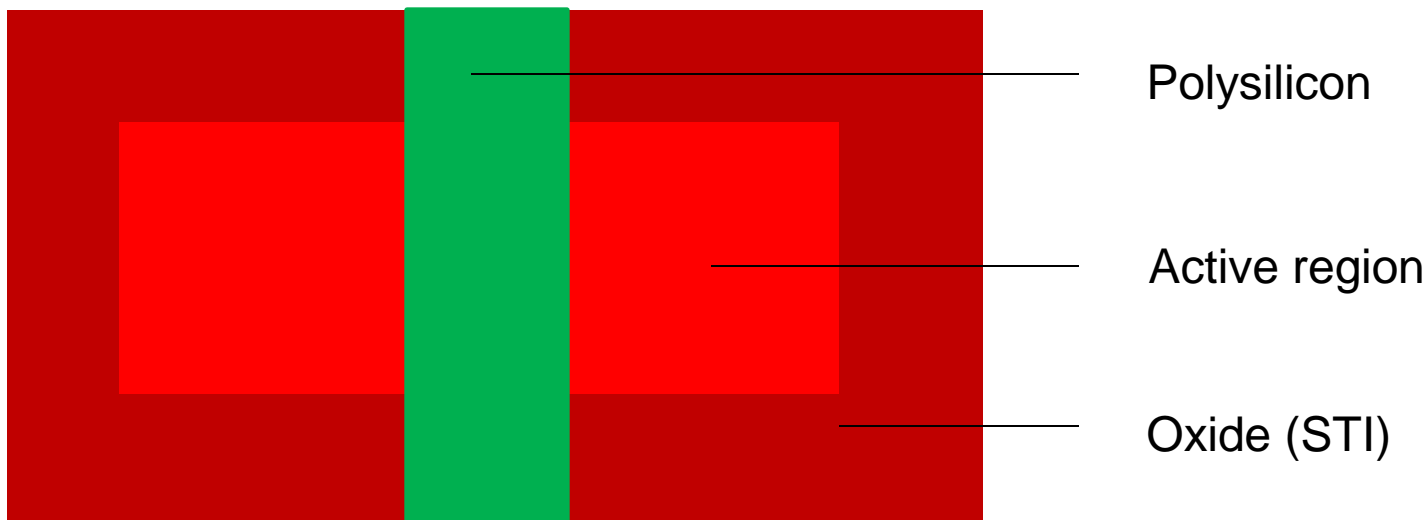
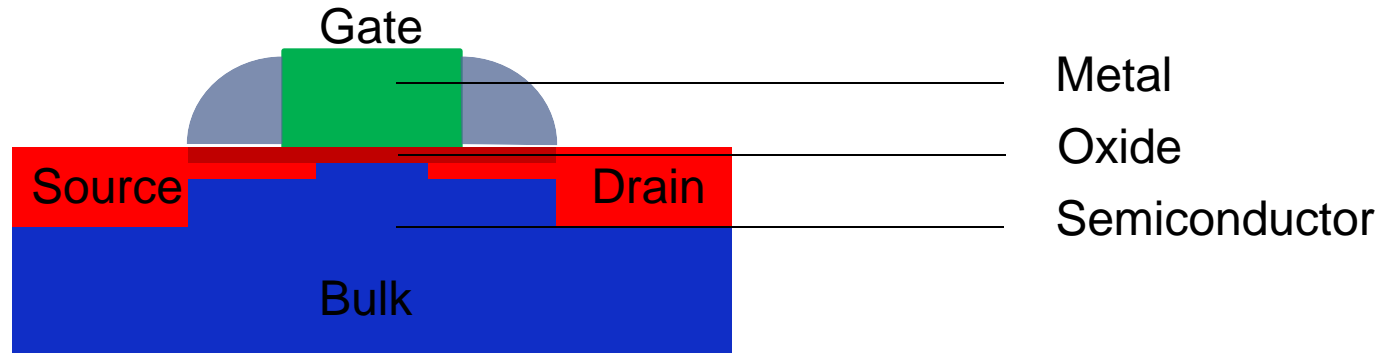


An introduction on MOSFET

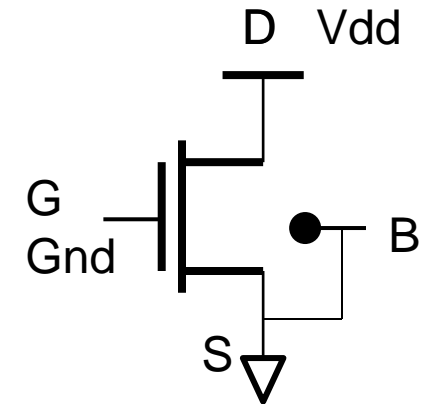
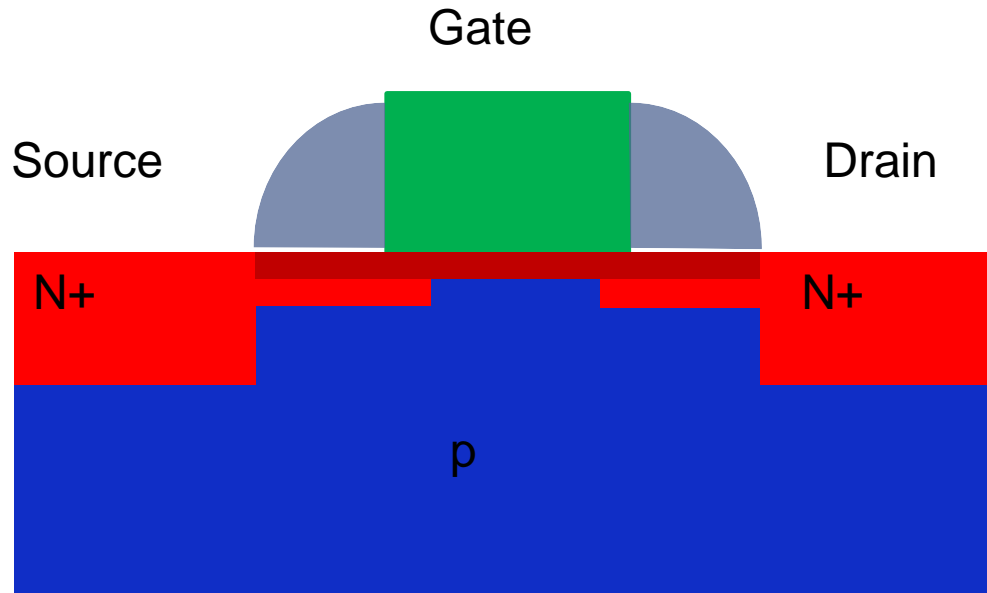
Outline

- MOSFET structure
- MOSFET operation
- Small dimension effects

MOS: Metal Oxide semiconductor

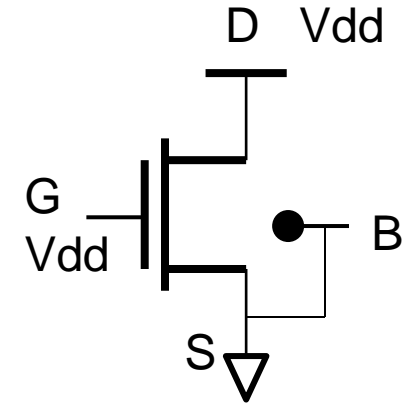
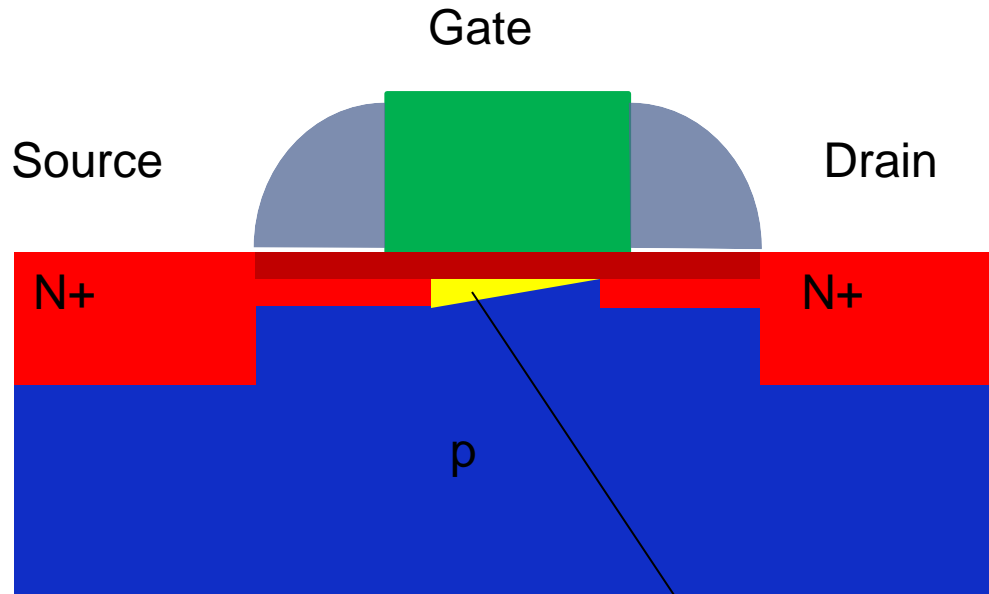


NMOS - off



- No inversion layer in channel.
- No drive (drift) current.
- Only leakage current (from gate and drain terminals).

NMOS – on (saturation)



- When $V_{gs} > V_{th}$, an inversion layer is formed.

Modes of operation

- Cutoff

- $(V_{gs} < V_{th})$

$$I_d = I_0 e^{\frac{V_{gs} - V_{th}}{nV_T}}$$

- Saturation

- $V_{GS} > V_{th}$
 $V_{DS} > (V_{GS} - V_{th})$

$$I_d = \frac{\mu_n C_{ox} W}{2L} (V_{gs} - V_{th})^2$$

- Linear region

- $V_{GS} > V_{th}$
 $V_{DS} < (V_{GS} - V_{th})$

$$I_d = \mu_n C_{ox} \frac{W}{L} \left((V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

Body effect

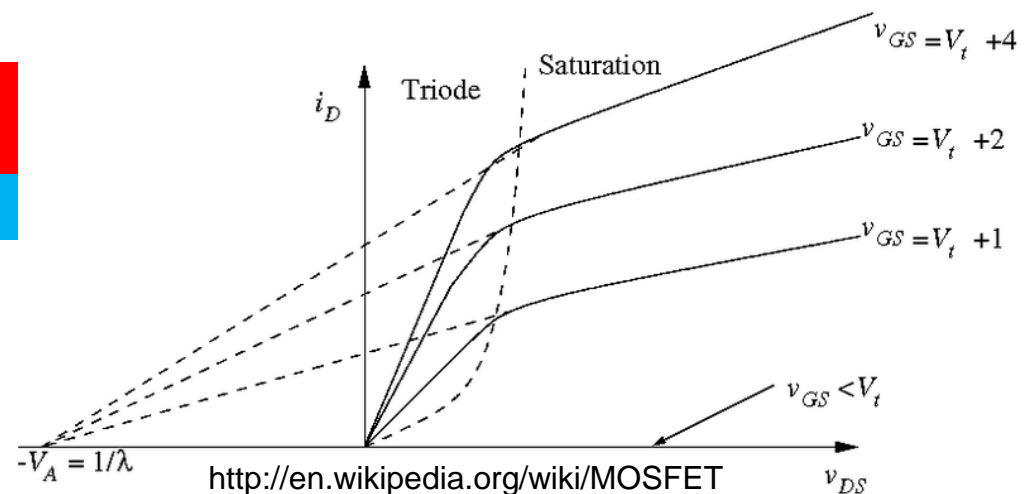
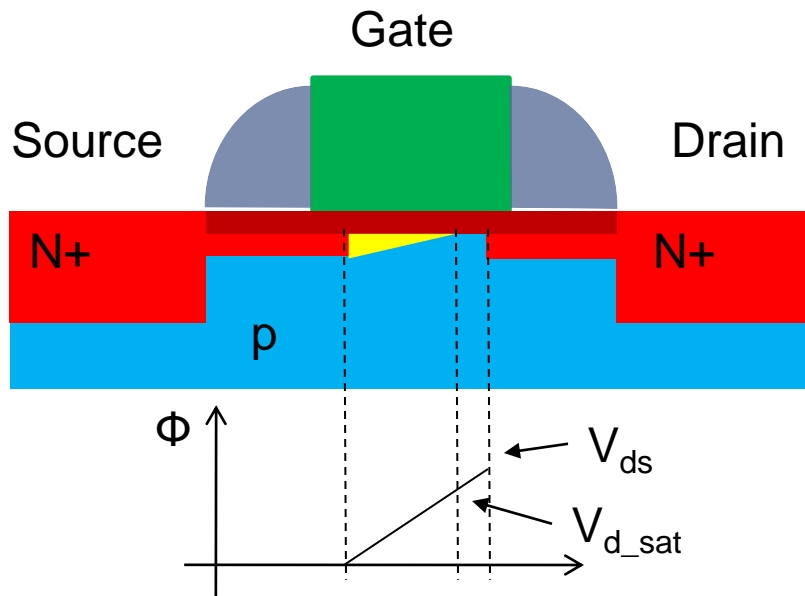
- $V_{th} = V_{th0} + \gamma [(V_{sb} + 2\Phi)^{0.5} - (2\Phi)^{0.5}]$

Channel length modulation

- L effective reduce when $V_d > V_{d_sat}$

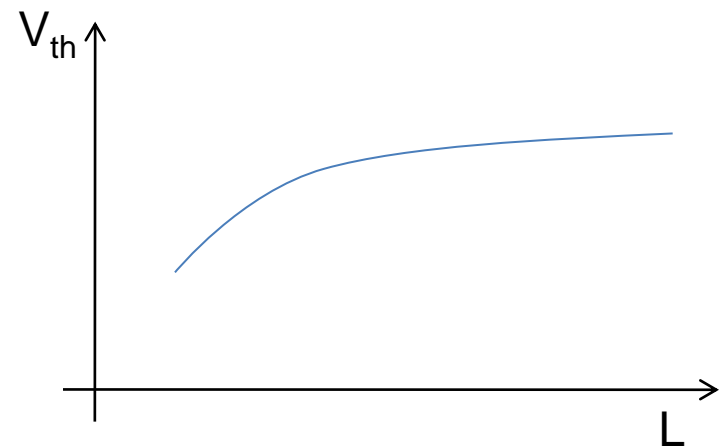
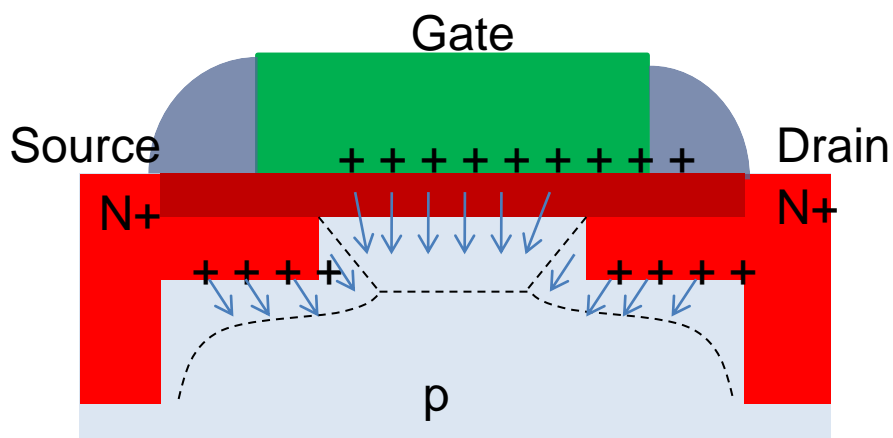
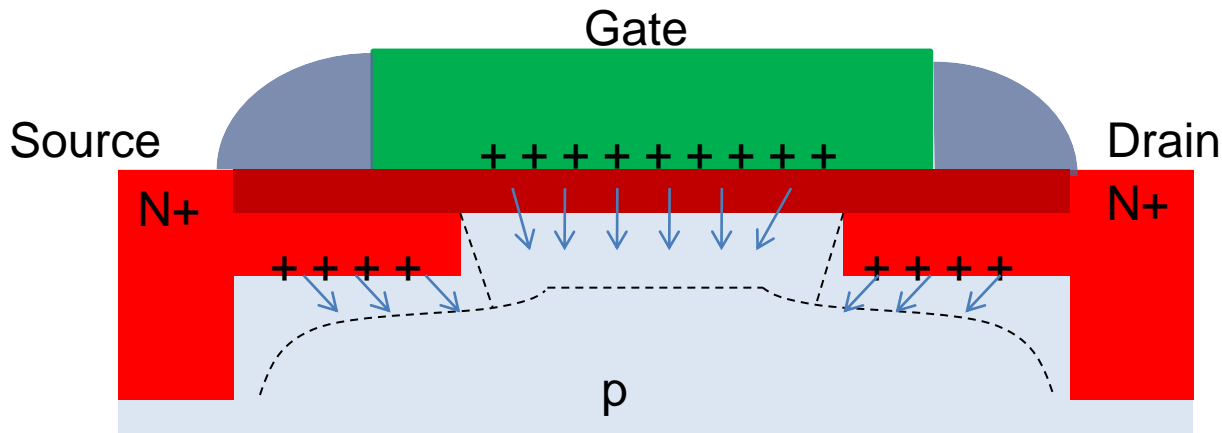
$$I_d = \frac{\mu_n C_{ox} W}{2L'} (V_{gs} - V_{th})^2, L' = L - \Delta L$$

$$I_d = I_{d_sat} \left(\frac{L}{L - \Delta L} \right) \approx I_{d_sat} \left(1 + \frac{\Delta L}{L} \right)$$



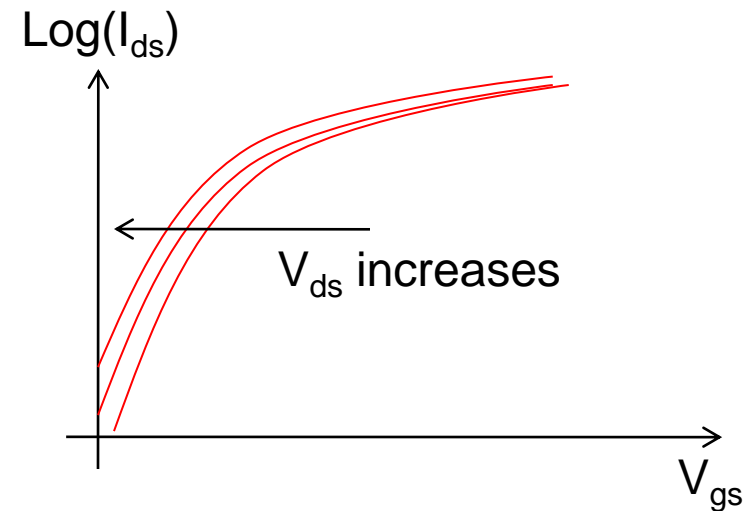
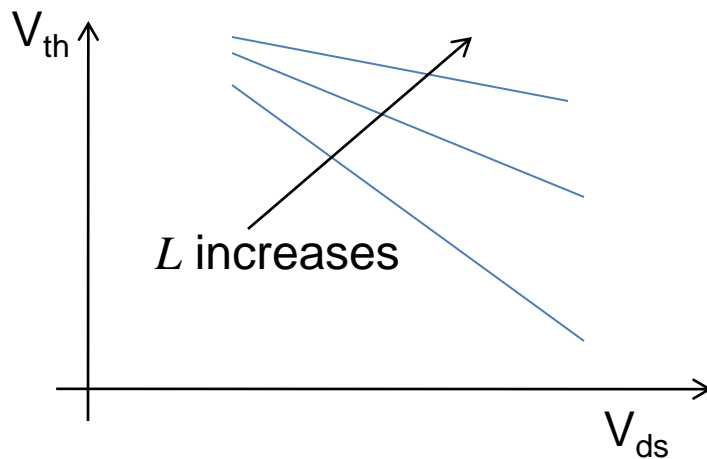
Short channel effects

- Charge sharing



Drain-induced barrier lowering (DIBL)

- Drain voltage “pull down” electron barrier.
- V_{th} depends on both L and V_{ds} .



Velocity saturation

$$v = \mu_{eff} E, \text{ Valid only when } E \ll E_{sat}$$

$$v = \frac{\mu_{eff} E}{(1 + E / E_{sat})}$$

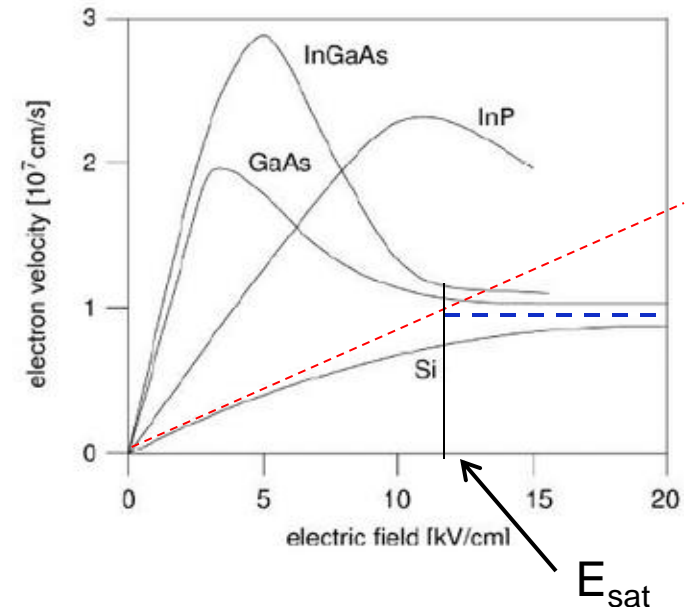
No velocity saturation

$$I_d = \mu_n C_{ox} \frac{W}{L} \left((V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right)$$

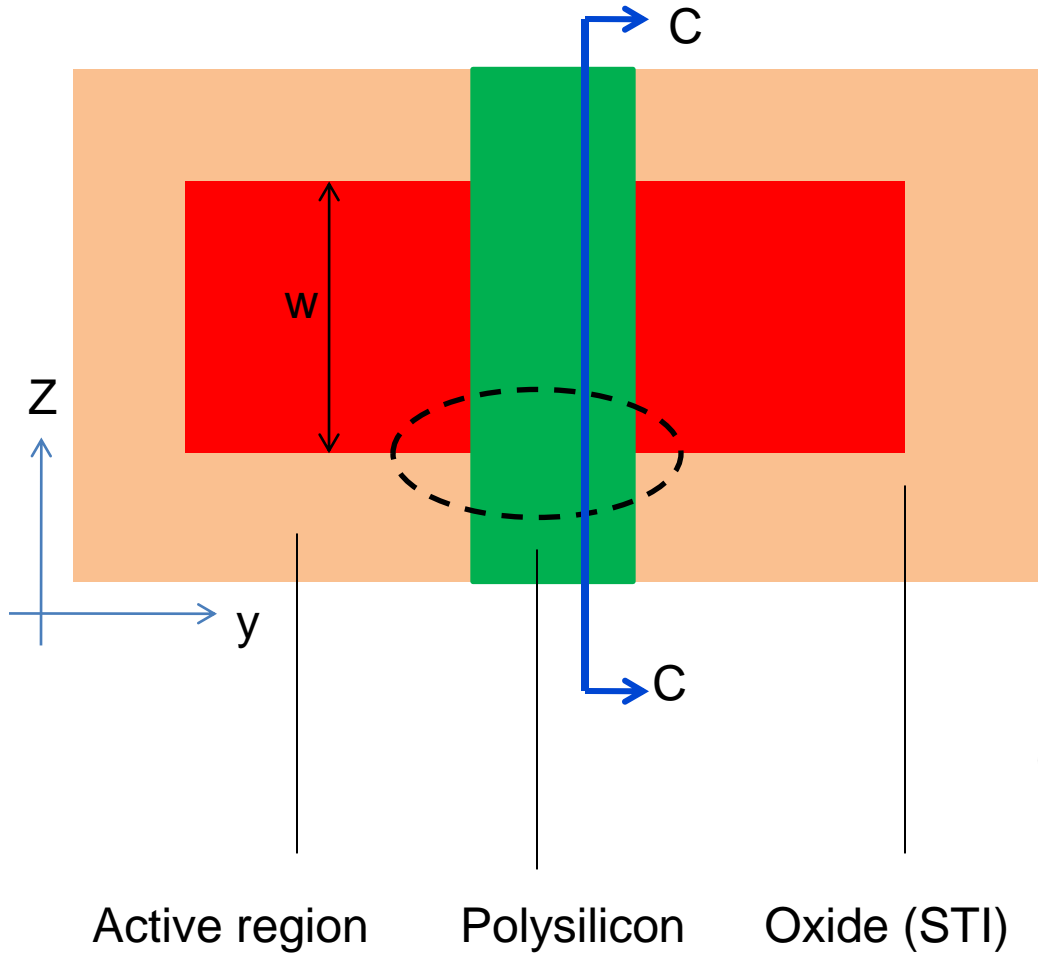
With velocity saturation***

$$I_d = \mu_{eff} C_{ox} \frac{W}{L} \left((V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right) \left(\frac{1}{1 + (V_{ds} / E_{sat} L)} \right)$$

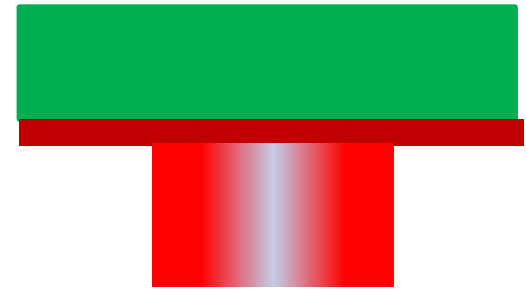
*** μ_{eff} and V_{th} are treated as constants across channel.



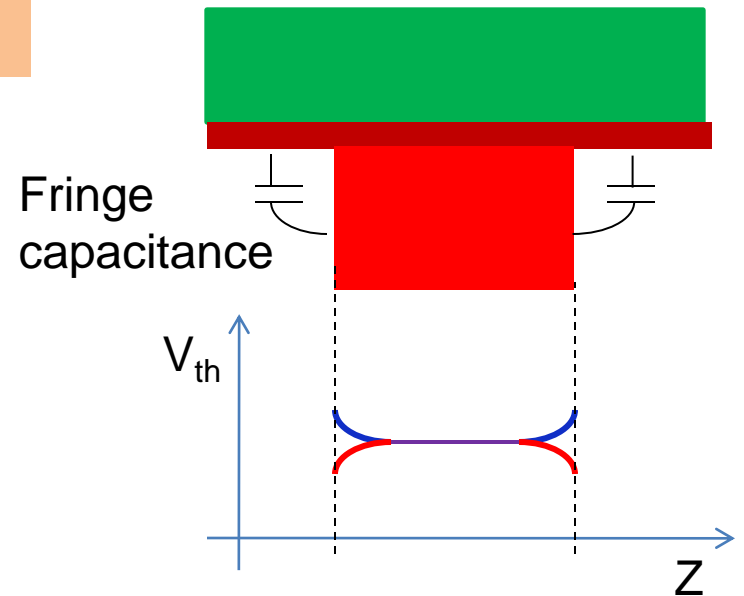
Narrow width effects



Cross section along C



Non-uniform doping



References

1. R. S. Muller, T. I. Kamins with M. Chan, “Device Electronics for Integrated Circuits”, 3rd edition, John Wiley & Sons, 2002.
2. Y.-M. Sheu, K.-W. Su, S. Tian, S.-J. Yang, C.-C. Wang, M.-J. Chen, *and S. Liu*, “Modeling the Well-Edge Proximity Effect in Highly Scaled MOSFETs”, IEEE Trans. On Electron Devices, vol. 53, no. 11, 2006.
3. K. Ohe, S. Odanaka, K. Moriyama, T. Hori, and G. Fuse, “Narrow-Width Effects of Shallow Trench-Isolated CMOS with n+-Polysilicon Gate”, IEEE Trans. On Electron Devices, vol. 36, no. 6, 1989.
4. C. Pacha, M. Bach, K.v. Arnim, R. Brederlow, D. S.-Landsiedel, P. Seegebrecht, J. Berthold, and R. Thewes, “Impact of STI-Induced Stress, Inverse Narrow Width Effect, and Statistical VTH Variations on Leakage Currents in 120 nm CMOS”,