

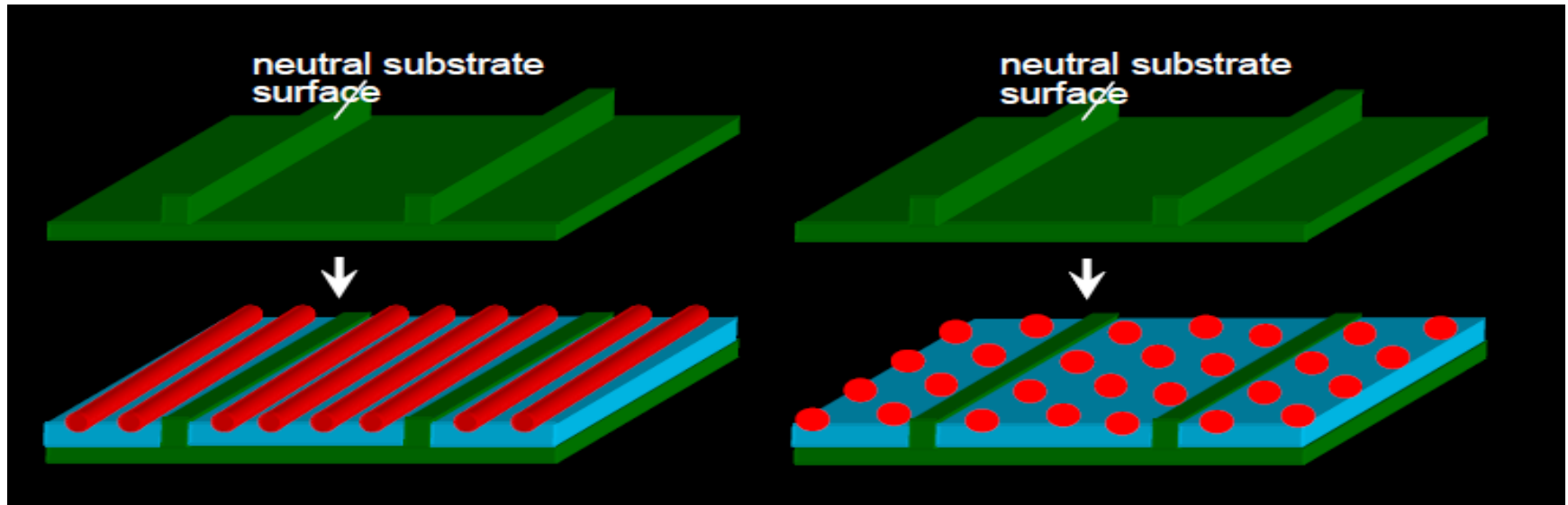
SPIE Advanced Lithography 2014 Highlights

Abde Ali Kagalwalla

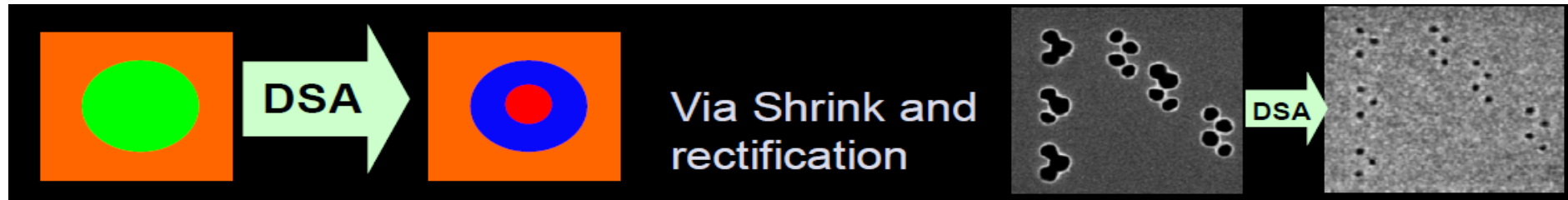
A Full-chip DSA Correction Framework

Wei-Long Wang, Azat Latypov, Yi Zou and
Tamer H. Coskun
Globalfoundries

Directed Self Assembly (DSA)



Source: Hinsberg, DSA Workshop, 2010



Goal of this paper is to find lithographically patterned guiding templates for random contact layer

Initial Solution Generation

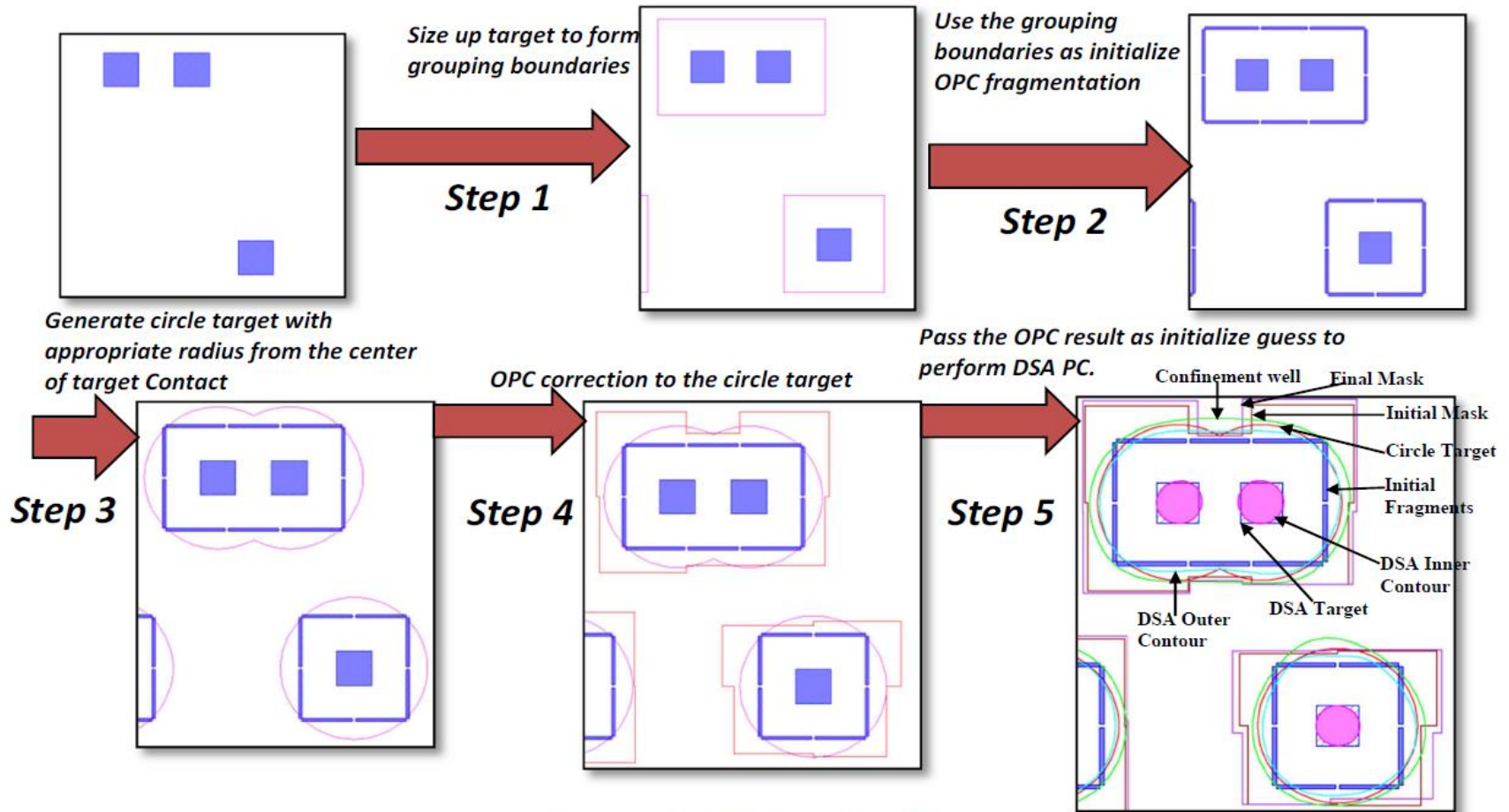
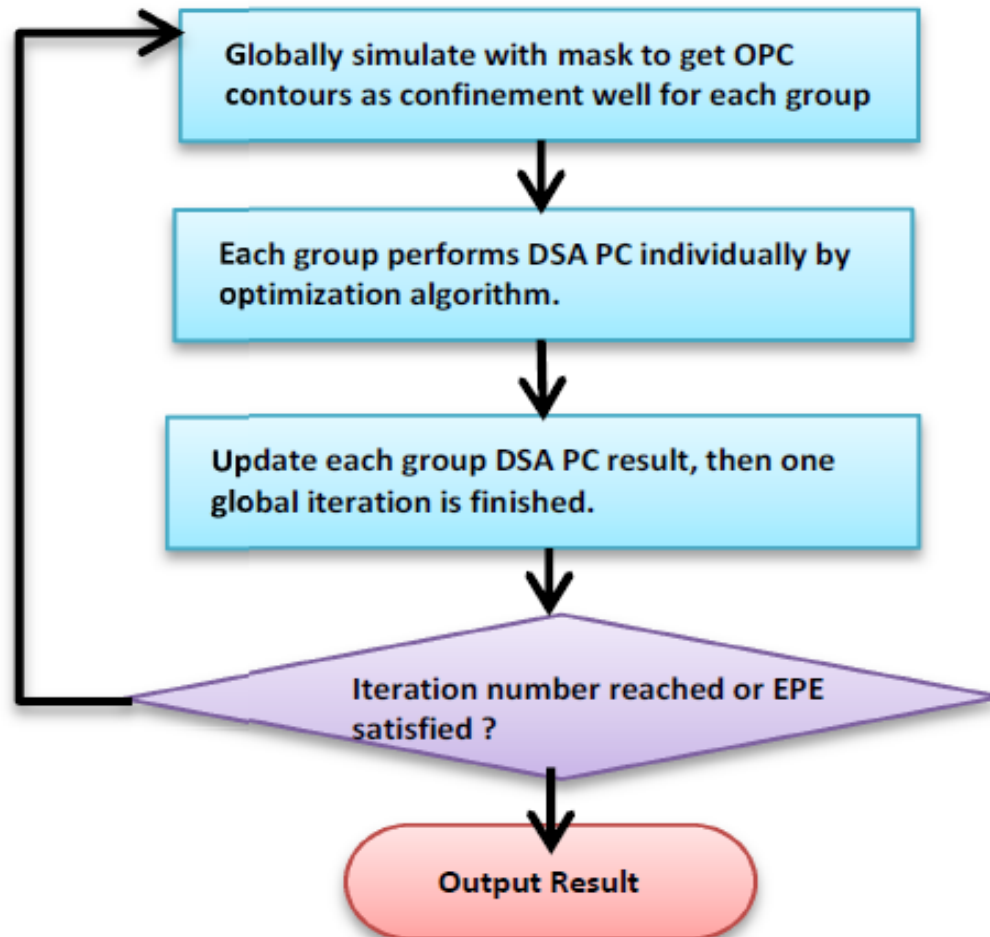


Figure 1: The DSA correction flow

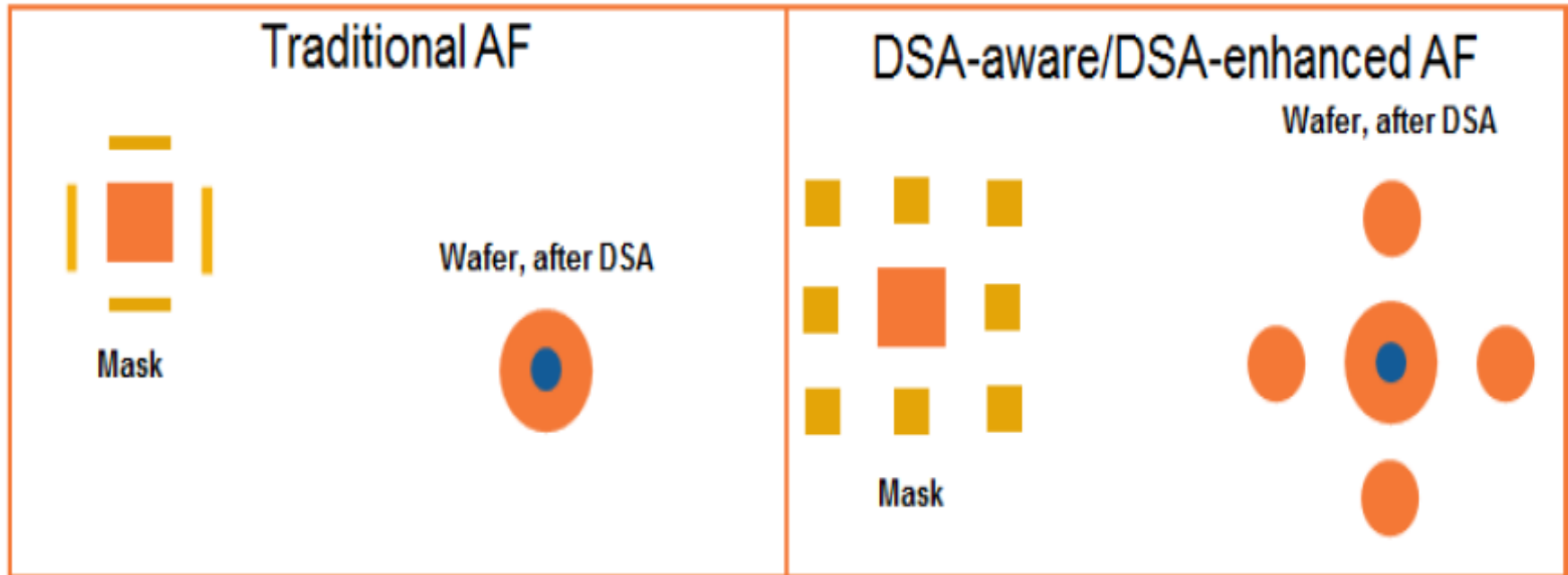
DSA-OPC Co-optimization

Edge fragments of template features moved to minimize EPE of final patterns after DSA

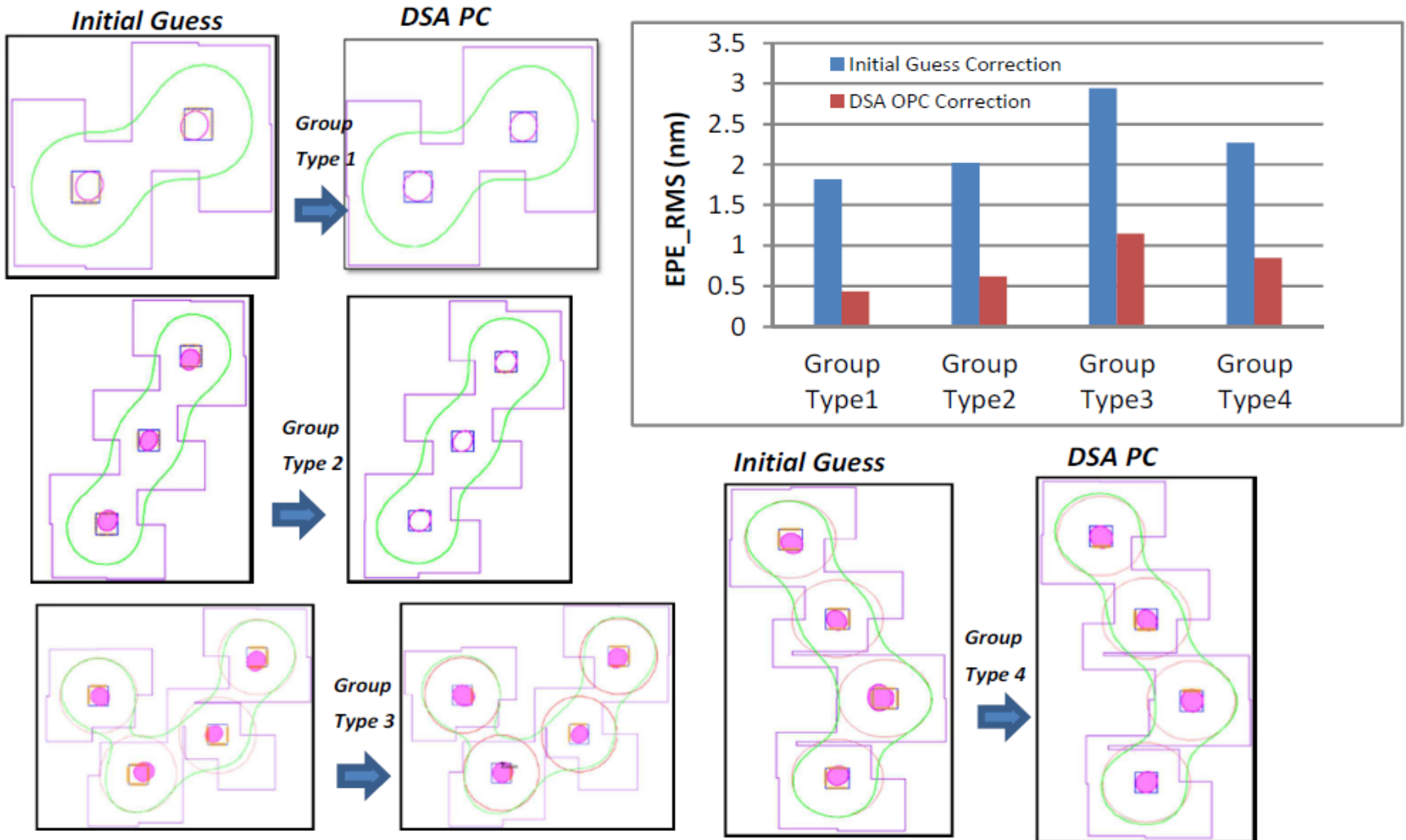


DSA-Aware Assist Feature Insertion

- In conventional lithography assist features must not print on wafer.
- With DSA, printable assist features can be used as long as BCP pattern is not etch transferrable.



Sample Simulation Results



Anti-Spacer Double Patterning

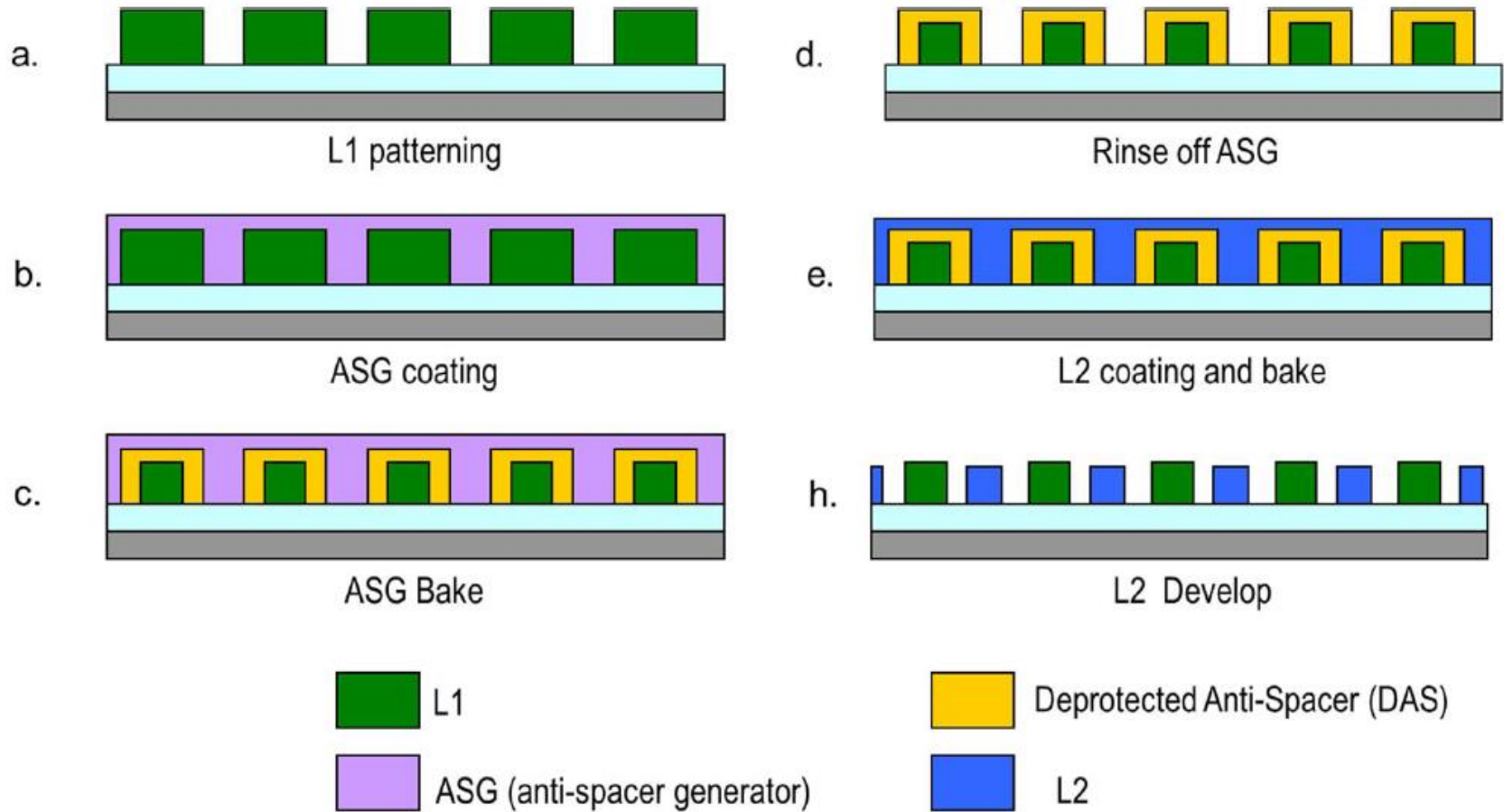
Michael Hyatt**, Karen Huang*, Anton DeVilliers***, Mark Slezak*, Zhi Liu*

*JSR Micro, Inc.

**Micron Technology, Inc.

***Tokyo Electron America, Inc.

Process Flow



Creating Asymmetric Design Target

- Useful for DRAM manufacturing, where SADP is unable to create asymmetric targets.

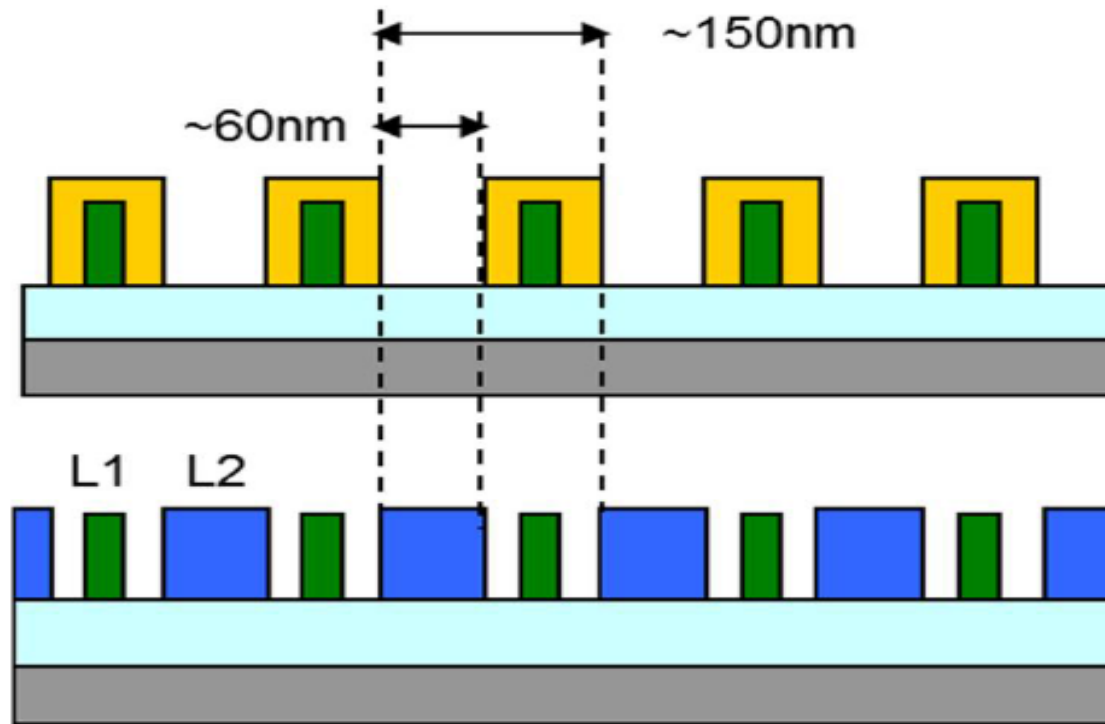
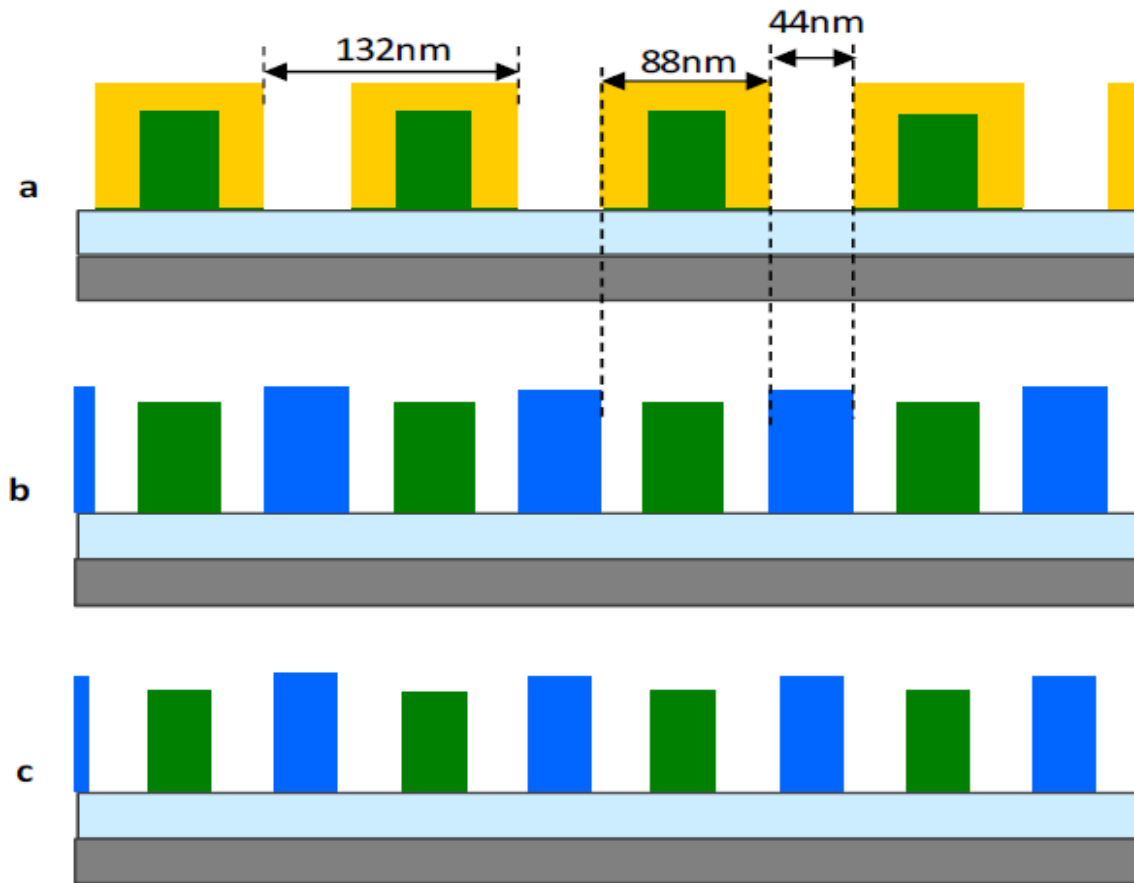


Figure 3.1.1 Asymmetric Design Target

CD Uniformity Challenge for ASDP Technology



	CD avg	3Sigma
L1	45.1 nm	4.0 nm
L2	47.2 nm	9.3 nm
Space	16.4 nm	5.1 nm

Figure 3.2.2 Symmetric design for equal line space imaging

(a) Post DAS formation (b) Post L2 develop (c) Post plasma trim