SPIE’11 Review

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Decomposition-Aware Standard Cell Design Flows to Enable DPT (IBM)

- DPT unavoidable below 80nm pitch
Design-Flow Components Affected by DPT

- Functional Requirements
- High-Level Design
- RTL design
- Functional Verification
- Synthesis, Gate-Level Netlist
  - Placement
  - Routing
- Chip Finishing
- Extraction, Timing, Signoff
- Tapeout
- Incoming Checks
- Design Services
- Data Preparation
- Mask Build
- Wafer Fabrication
- Test and Characterization

Standard Cell Library

Process Design Kit:
- Design Rules
- Device Models
- Interconnect Models

Process Assumptions

Design
Technology
DP Decomposition and Issues

- Need DP decomposition that will eliminate layout legalization inefficiency
  - Decomposition for easy-to-fix conflicts (work in progress)
DP Placement – Extreme approaches

- No abutment rules:
  - conflicts avoided with smart placement
  - arbitrary placement guaranteed to be clean

15% area overhead with 50% logic-cell util

too complicated
too conservative
DP Placement – Hybrid Approaches

1. Only worry about conflicts at vertical boundary, by either filler cells or flipping color (if possible)
2. Power pre-assigned, cell right forced to one color, flippable color w.r.t. power
   - Post-placement coloring or have two versions for each cell and placer chooses

As low as 2-3% area overhead

Some infeasible cells, need large cell-height
DP Routing

• Typical iterative optimization involving cycles of coloring, checking, locally re-routing, re-coloring, and re-checking.

• “To avoid additional routing complexity from DPT, initial design flows will prevent routers from sharing wiring levels that are used predominantly in the cell level design.” (also with globalfoundries)
  – Eliminates DPT specific cell-to-router issues
  – May not be a long term solution
SADP Friendly Detailed Routing \textit{(Mentor)}

- RMT bits
- Routing variable (R):
  - 1 $\rightarrow$ already occupied and routing blockage grids
- Mandrel-blocked variable (M):
  - 1 $\rightarrow$ conflicting on mandrel
- Trim-blocked variable (T):
  - 1 $\rightarrow$ conflicting on trim
Some Details

- **Protective grid**: trim grids that can provide assist spacer if filled with mandrel.
- **Bare grid**: occupied trim grid is bare if its protective grids are “don’t cares”. Assign to trim or mandrel?
- Calculate hesitation parameters for each grid (likelihood).
- Heuristic to find path with best cost for each net (min WL, WL on each mask).

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<th>Design</th>
<th>Area ($\mu m^2$)</th>
<th>Nets</th>
<th>Router</th>
<th>Wirelength (nm)</th>
<th>SADP statistics (nm)</th>
<th>Runtime (sec.)</th>
<th>Ratio</th>
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Double Patterning Compliant Logic Design (Globalfoundries, cadence, AM)

- 1900i cheaper less overlay accuracy
- 1950i slightly better throughput → almost same cost
- Spacer deposition → $14-$22 more per 12” wafer for 4 metal layers
  - Need 0.5%-1% less die area for same overall cost