Power Gating Implementation in SoCs

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Dynamic vs. Leakage Power Components of IC Power

Source: ITRS Roadmap 2007

- Dynamic Power
- Leakage Power
- Sub-Threshold Leakage
- Gate-Oxide Leakage
- Possible trajectory for high-k dielectrics
- Cross-Over

Power Consumption vs. Physical Gate Length [nm]

- 1990
- 1995
- 2000
- 2005
- 2010
- 2015
- 2020
Motivation

• Battery Life.
• Cost of packaging and cooling.
• Reliability and Performance degradation.
  – Slower, leakier circuits at high temperatures, higher rate of electromigration etc.
• More features being integrated on smaller area.
• Leakage Power may soon become the dominating part of total power consumption
Low Power Techniques for SoCs

• Parallelism and Pipelining.
• Gate sizing
• Multi Vdd
• Clock Gating
• Power Gating
• DVFS
• Device level techniques (high-k Hf based MOS)
Contribution of leakage power

Example: ASICs [source: STMicroelectronics].

Example: Microprocessors [source: Intel].

Itanium 2:
180nm, 1.5V, 1.0GHz,
221MTx (core+cache)

Itanium 3:
130nm, 1.3V, 1.5GHz,
410MTx (core+cache)
Power gating

“The basic strategy of power gating is to provide two power modes: a low power mode and an active mode. The goal is to switch between these modes at the appropriate time and in the appropriate manner to maximize power savings while minimizing the impact to performance.”
Activity Profile with No Power Gating

No Power Gating

Power Gating Implemented

Realistic Power Gating

Ref [2]. LPMM
Block Diagram of SoC with power Gating

Ref [2]. LPMM
Headers and Footer Switches

Only Headers or Footers used in design sub 90nm (IR drop)
Switch Sizing Considerations

- Smaller switches ➔ smaller area, larger resistance, good leakage reduction
- Bigger Switches ➔ larger area, smaller resistance, relatively low leakage reduction.

[Ref: J. Frenkil, Springer’07]
Switch Placing Architectures (Physical Design)

• Switch in Cell: Switch transistor in each standard cell. (Area, Physical Design ease).

• Grid of Switches: Switches placed in an array across the power gated block. 3 rails routed through the logic block. (Power, Gnd, Virtual)

[Ref: S. Kosonocky, ISLPED'01]
Switch Placing Architectures (Physical Design) .. contd

- Ring of switches: Used primarily for legacy designs where the physical design of the block may not be disturbed.
Signal Isolation

• Powering down the region will not result in crowbar current in any inputs of powered up blocks.

• None of the floating outputs of the power-down block will result in spurious behavior in the power-up blocks.

Clamps add delay!
State Retention

• While Logic Block power Gating, we have to retain some critical register contents (FSM states).
• Saving and restoring state quickly and efficiently ➔ faster and power-efficient method to get the block fully functional after power up.
• DSP Unit – data flow driven – can start from reset on new data input.
• A cached processor – large residual state
State Retention Techniques

• **Software based register read writes.**
  Slow and increases active-sleep-active latency.
  Bus conflicts cause non-deterministic save/restore times.

• **A scan-based approach based on using scan chains to store state off chip.**
  No area overhead as existing scan chains may be used,
  During power down, scan registers are routed to memory.
  During power up scan chains are loaded from memory.

• **Retention registers**
  Area overhead, typically 20% or more.
Retention Registers
Power gating Design Verification

- Verilog and other HDLs do not provide for specifying power connections at RTL.
- UPF (unified power format) specifies simulation semantics and language format for PG.
- Key Simulator Requirements:
  - Functional modeling of power gating, isolation and retention.
Design for Test Implications

- External controls and observability of power gating signals.
- PDN testing for correct behavior.
- Testing PG controller, retention and isolation behavior
Power Gating Considerations

• Library design: special cells are needed
  Switches, isolation cells, state retention flip-flops (SRFFs)

• Headers or Footers?
  Headers better for gate leakage reduction, but ~ 2X larger

• Which modules, and how many, to be power gated?
  Sleep control signal must be available, or must be created

• State retention: which registers must retain state?
  Large area overhead for using SRFFs

• Floating signal prevention
  Power-gate outputs that drive always-on blocks must not float

• Rush currents and wake-up time
  Rush currents must settle quickly and not disrupt circuit operation

• Delay effects and timing verification
  Switches affect source voltages which affect delays

• Power-up & power-down sequencing
  Controller must be designed and sequencing verified
Power Gating Flow

- Design power-gating library cells
- Determine which blocks to power gate
- Determine state retention mechanism
- Determine rush current control scheme
- Design power-gating controller
- Power gating aware synthesis
- Determine floorplan
- Power gating aware placement
- Clock tree synthesis
- Route
- Verify virtual-rail electrical characteristics
- Verify timing
## Full Power Gating Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Design</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A</td>
</tr>
<tr>
<td>Process technology</td>
<td>90nm</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.5V</td>
</tr>
<tr>
<td>Logic function</td>
<td>32-bit ALU</td>
</tr>
<tr>
<td>Retain state in registers?</td>
<td>yes</td>
</tr>
<tr>
<td># of instances</td>
<td>1,852</td>
</tr>
<tr>
<td># of power-gated logic instances</td>
<td>1,388</td>
</tr>
<tr>
<td># of switch instances</td>
<td>104</td>
</tr>
<tr>
<td># of interface instances</td>
<td>206</td>
</tr>
<tr>
<td>Logic cell to switch cell ratio</td>
<td>13.3</td>
</tr>
<tr>
<td>Power-gated logic cell area (um²)</td>
<td>15,259</td>
</tr>
<tr>
<td>Switch cell area (um²)</td>
<td>2,565</td>
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<tr>
<td>Switch area overhead (%)</td>
<td>16.8%</td>
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<tr>
<td>Interface cell area (um²)</td>
<td>791</td>
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<tr>
<td>Interface cell area overhead (%)</td>
<td>5.2%</td>
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<tr>
<td>Original bounding-box area (um²)</td>
<td>977,725</td>
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<tr>
<td>New bounding-box area (um²)</td>
<td>977,725</td>
</tr>
<tr>
<td>Bounding-box area increase (%)</td>
<td>0.0%</td>
</tr>
</tbody>
</table>

Ref: Chinnery, Keutzer et al. [1]
## Selective Power Gating Results

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<thead>
<tr>
<th>Parameter</th>
<th>Design</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process technology</strong></td>
<td>A 90nm</td>
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<tr>
<td><strong>Supply voltage</strong></td>
<td>1.5V</td>
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<tr>
<td><strong>Logic function</strong></td>
<td>32 bit ALU</td>
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<td><strong>Retain state in registers?</strong></td>
<td>yes</td>
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<td><strong># of instances</strong></td>
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<tr>
<td><strong># of power-gated logic instances</strong></td>
<td>359</td>
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<td><strong># of switch instances</strong></td>
<td>55</td>
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<tr>
<td><strong># of interface instances</strong></td>
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<tr>
<td><strong>Logic cell to switch cell ratio</strong></td>
<td>6.5</td>
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<tr>
<td><strong>Power-gated logic cell area (um²)</strong></td>
<td>6.136</td>
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<tr>
<td><strong>Switch cell area (um²)</strong></td>
<td>1,192</td>
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<tr>
<td><strong>Switch area overhead (%)</strong></td>
<td>19.4%</td>
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<td><strong>Interface cell area (um²)</strong></td>
<td>791</td>
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<tr>
<td><strong>Interface cell area overhead (%)</strong></td>
<td>12.9%</td>
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<tr>
<td><strong>Original bounding-box area (um²)</strong></td>
<td>977,725</td>
</tr>
<tr>
<td><strong>New bounding-box area (um²)</strong></td>
<td>977,725</td>
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<tr>
<td><strong>Bounding-box area increase (%)</strong></td>
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References

[3] Low Power Design Methodologies and Flow. – Frenkil and Rabaey