ERSA: Error-Resilient System Architecture

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Outline

- Probabilistic Applications
- ERSA Overview
- SRC and RRC
- ERSA experiments
Probabilistic Applications

• Some probabilistic applications such as Recognition, Mining and Synthesis (RMS) applications have the following properties:
  – Massive parallelism
  – Algorithmic resilience (e.g. iterative refinement, relying on convergence)
  – Cognitive resilience (e.g. qualitative results, )

• Key Challenges:
  – Control flow is hardly error-tolerant
  – Asymmetric tolerance: low-order bits vs. high-order bits
  – Surviving from high error rates
Hardware Architecture

Super Reliable Core
- Highly Reliable Main thread (Fig. 3)
- OS visible
- Supervise RRCs

Relaxed Reliability Core
- Inexpensive & Unreliable Worker thread (Fig. 3)
- Sequestered from OS
- Reliable MMU, restart unit

The diagram illustrates the hardware architecture with various components and their interconnections. The reliable components are indicated by a box, while the unreliable components are marked in red.
Super Reliable Core (SRC)

- An SRC is responsible for:
  1. Executing non-error-tolerant codes
     - OS
     - Application main thread
  2. Supervising RRC
     - Workload distribution
     - Sanity checks
     - Timeout / Reset
     - Computation results checking
Relaxed Reliability Core (RRC)

- RRC is the main execution units that can be unreliable
  - A reliable memory management unit is used to detect memory access bound violations
Computation Model
Software Optimization

• Convergence Damping
  – If $\Delta > \text{threshold}$, let $\Delta = \text{threshold}$

• Convergence Filtering
  – If $\Delta_i > \text{threshold}$, discard $\Delta_i$
Experiment Platform

- 2 Processor cores in FPGA
  - One for SRC
  - One for RRC with time-multiplexing
- Bit-error in injected randomly in registers
  - 32 general purpose registers
  - Stack and base pointers
Results

Figure 5. ERSA computation accuracy. Basic ERSA and Enhanced ERSA implementations are compared.