E-Beam Direct Write

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NanoCAD Group Meeting 03/10/10
EBDW Motivation

- EUV: -- high CoO → might be suitable only for high-volume
  -- Unable to reach acceptable throughput
- Mask cost threatening the profitability of scaling
- EBDW: accurate printability and maskless!

% of wafer cost that mask costs represent

<table>
<thead>
<tr>
<th></th>
<th>250nm</th>
<th>130nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASIC</td>
<td>32%</td>
<td>56%</td>
</tr>
<tr>
<td>DRAM</td>
<td>7%</td>
<td>10%</td>
</tr>
<tr>
<td>Logic</td>
<td>12%</td>
<td>24%</td>
</tr>
</tbody>
</table>

Source: IC Knowledge

Source: Maruyama EIPBN’09
VSB vs. Character Projection

Source: Sugihara ISCAS’06
VSB vs. Character Projection

Variable Shape Beam (VSB) vs. Character Projection (CP)

Source: ebeam.org
Aperture Misalignment

- CP unaffected by apertures misalignment

Source: ebeam.org
Shot Count

• Design for E-Beam
  – Co-designing the cell library and the stencil mask
  – Optimizing the physical design for CP

Source: ebeam.org
Throughput for Small Volume

Source: Maruyama EIPBN’09
Limited Character Size

- Electrons in an e-beam repel each other
- As an e-beam becomes larger, printed image gets more blurred
- Use close to maximum allowed e-beam

Entire Flip-flop in 1 shot is possible

Source: ebeam.org
Limited Number of Characters

Advantest

Previous specification of the F3000 character block with 100 characters

Source: A. Fijumura
ICCAD’09

The Packed Stencil allows, for example, this packed layout of 220-280 characters

Up to 12 character blocks

Up to 20 character blocks
Minimizing the Number of Characters

• Common Component as a character
• One cell can be printed using multiple shots of the same base character

Source: A. Fijumura
ICCAD’09
Minimizing the Number of Characters

- Large character is placed on a stencil
- Partial CP conversion to create smaller cells
  - Misalignment issues

<table>
<thead>
<tr>
<th>Logic Symbol</th>
<th>Projected Circuit image on wafer</th>
<th>Partial CP Conversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Large Buffer</td>
<td><img src="image" alt="Large Buffer Diagram" /></td>
<td><img src="image" alt="Large Buffer CP Conversion" /></td>
</tr>
<tr>
<td>Middle Buffer</td>
<td><img src="image" alt="Middle Buffer Diagram" /></td>
<td><img src="image" alt="Middle Buffer CP Conversion" /></td>
</tr>
<tr>
<td>Small Buffer</td>
<td><img src="image" alt="Small Buffer Diagram" /></td>
<td><img src="image" alt="Small Buffer CP Conversion" /></td>
</tr>
</tbody>
</table>

Source: Maruyama EIPBN’09
Design for E-Beam

- Optimize shot count at every SP&R step
- Allow only discrete metal widths
- Arrange some cells in one direction for less characters (e.g., SRAM)
- Avoid M1 stub routing
- Enclose via geometries completely inside standard cell pins

14 CP shots (Preferred)

14 CP shots + VSB shots (Avoid)

Source: ebeam.org
65nm Test Chip

Chip-A floor plan with DFEB library
Chip size = 4.2mm*8.4mm

Chip-B Floor plan with original library
Chip size = 4.2mm*8.4mm

1. Process: Fujitsu 65nm CMOS, 7 layer metal
2. Chip size: 4.2mm*8.4mm
3. VDD: 1.20v for core, 3.3v for IO
4. Clock: 166MHz, 162MHz and 33.3MHz
5. Random Logic size: 3+Mgates
6. Memory size: 786Kbit

Standard-cell lib

<table>
<thead>
<tr>
<th>Total cell count</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFEB</td>
</tr>
<tr>
<td>142</td>
</tr>
</tbody>
</table>

Source: Maruyama EIPBN’09
Character Layouts

Diffusion (active)

Poly

Metal-1

Contact

Source: Maruyama EIPBN’09
Area Overhead and Exposure Time

10x avg reduction in shot count compared to VSB (20x for poly)

< 4% chip-area overhead

Source: Maruyama EIPBN’09
Future Directions

• Combine DFEB with Multi-Column Cell E-beam
  – Extension of character set
  – Throughput enhancement

Source: Maruyama EIPBN’09