Adiabatic Logic

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A major part of the contents is from Reference 1

Terminology

- **Reversible logic**:
  - circuits that have **one-to-one** mapping between vectors of inputs and outputs
- "**Adiabatic**" : from thermodynamics
  - Process in which there is no exchange of heat with the environment

History

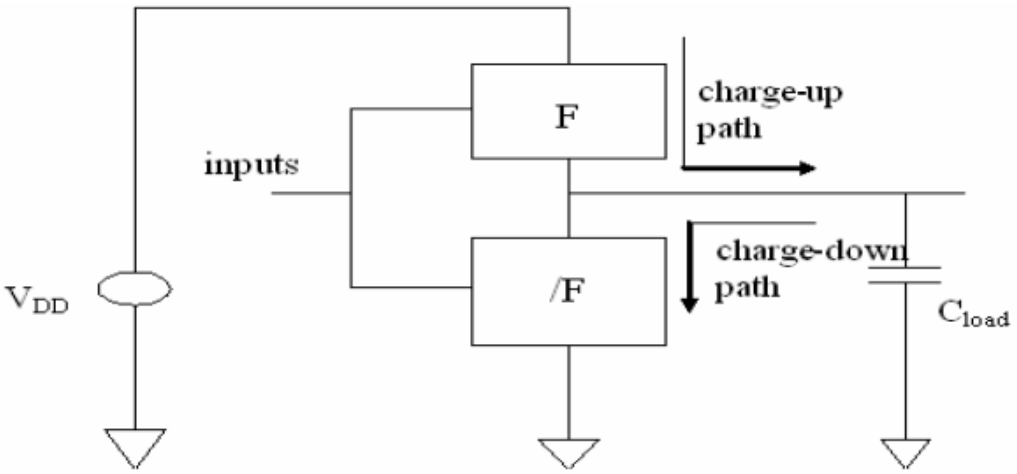
- Landauer (1961):
  - Logically irreversible operations in a physical computer necessarily dissipate energy
  - Logically reversible operations “can” be performed without dissipation
- Later, found that that a gate can work **energetically reversible** without the need to be **logically reversible**.

Adiabetic Circuits

- Energy reused rather than just dissipated
- Power advantage

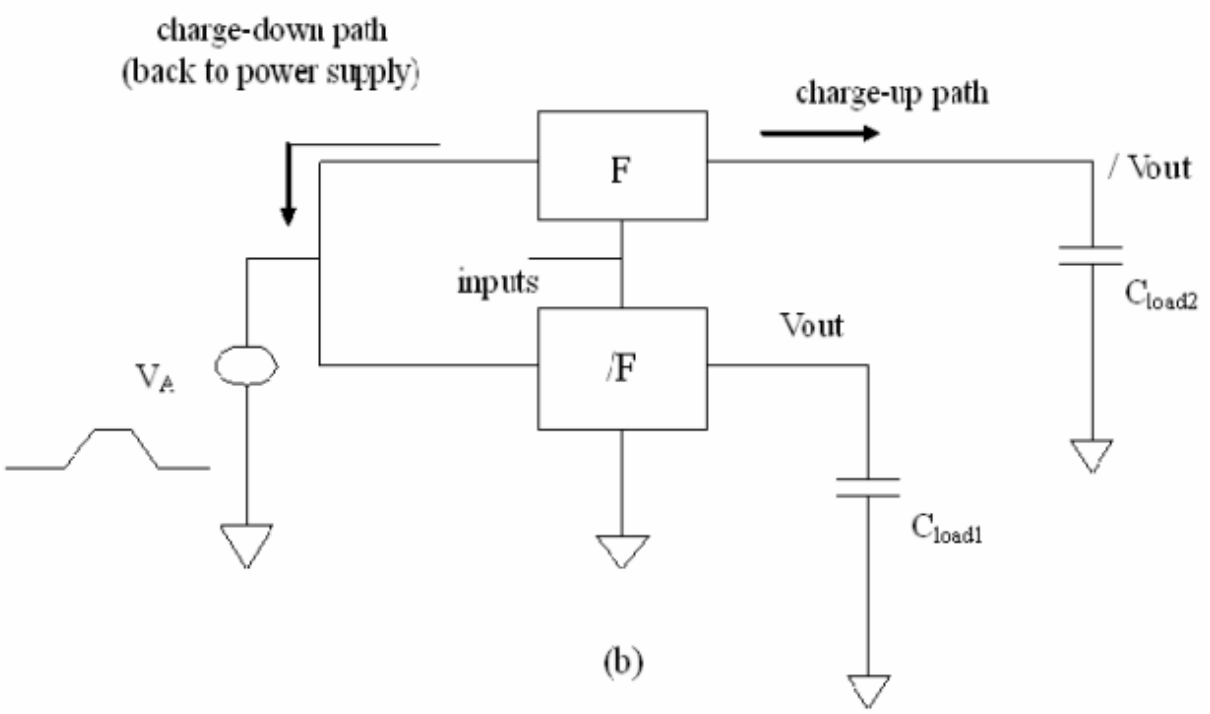
Conventional CMOS

- **Constant voltage**
- Energy dissipated per transition $=CV_{dd}^2/2$
  - Pull up: energy dissipated on PMOS
  - Pull down: charge dissipated via NMOS to ground
- Energy used only once



Adiabatic Logic

- Supply is a **power clock** (ramp)
- Pull down path: to **power supply**



Adiabatic Logic Energy Dissipation

- i(t)=c dV/dt

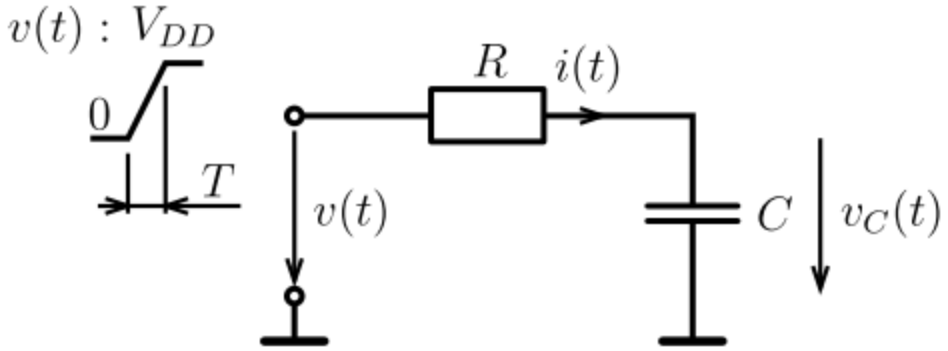
  =c Vdd/T

  (**Constant Current**)

- Energy during transition time T

  = I^2*R*T

  = R* C^2 * V_{dd}^2/T



Equivalent circuit

CMOS

- Dissipated energy in pull up and pull down
  = CV_{dd}^2
- Depends on C and Vdd only

Adiabatic

- Dissipated energy in charge and recovery
  = $2*R*C^2*V_{dd}^2/T$
- Depends on **size** of transistor and **T** as well
- Slower circuit is charged➔ less energy dissipation

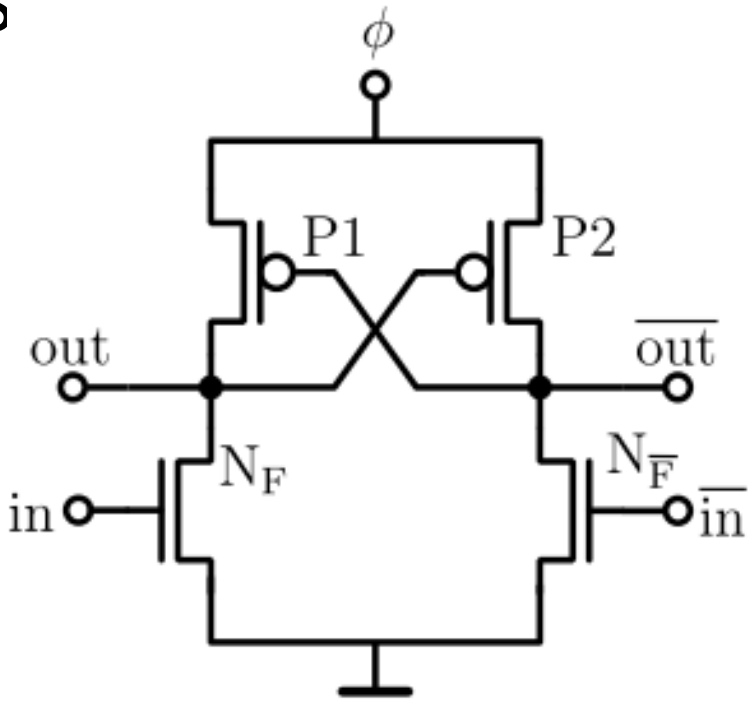
T>2RC ➔ Adiabatic has less energy dissipation if we assume activity factor of 1

Adiabatic Logic Families

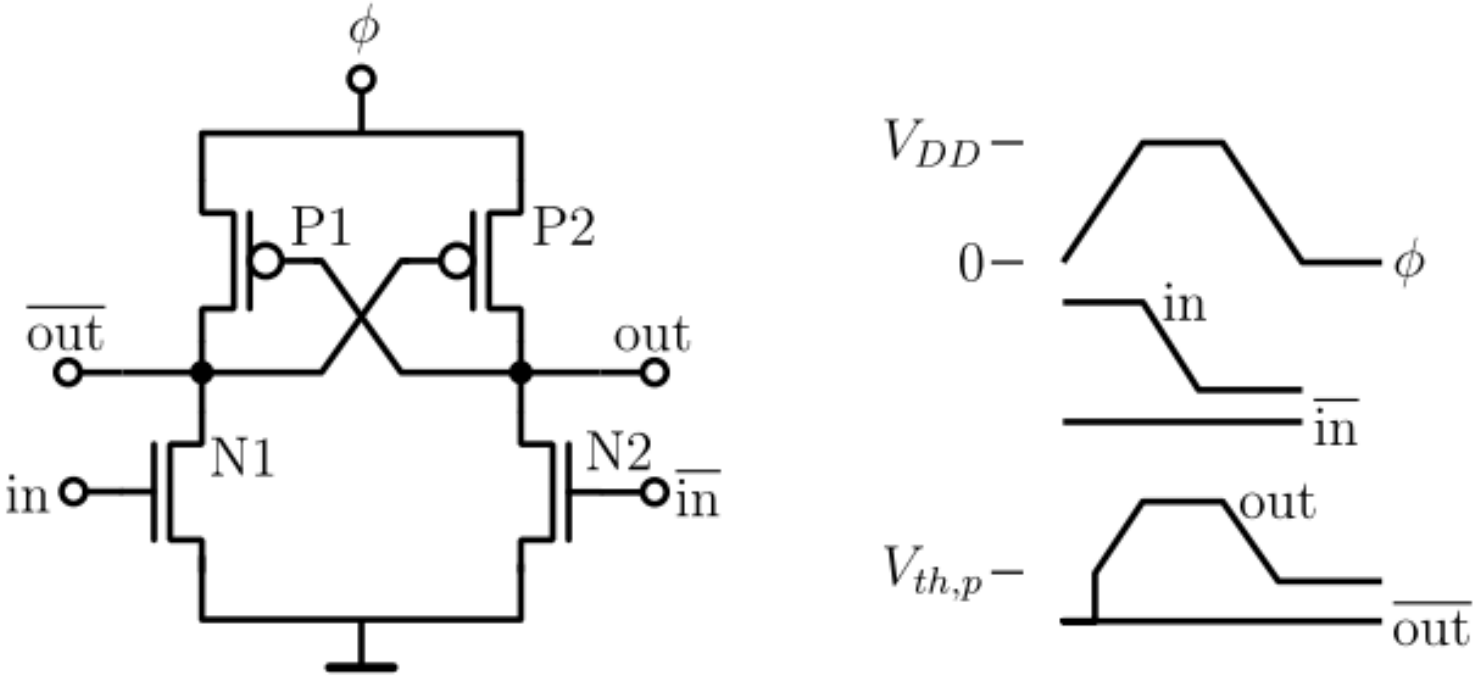
- Adiabatic system has:
  - *Digital core*: adiabatic gates
  - *Generator* of *power clock* signals
    - 4-phase power clock for cascaded gates
    - Efficient generation essential for high energy saving factor
- Two of the most popular
  - Efficient Charge Recovery Logic (ECRL)
  - Positive Feedback Adiabatic Logic (PFAL)

1-ECRL Inverter

- Logic implemented using NMOS
- 2 cross coupled PMOS to store info
- For a different function e.g. NAND
  - a series connection of 2 NMOS instead of N_F, using A and B as input s.
  - 2 parallel transistors, having A' an B' as inputs instead of $N_{F'}$



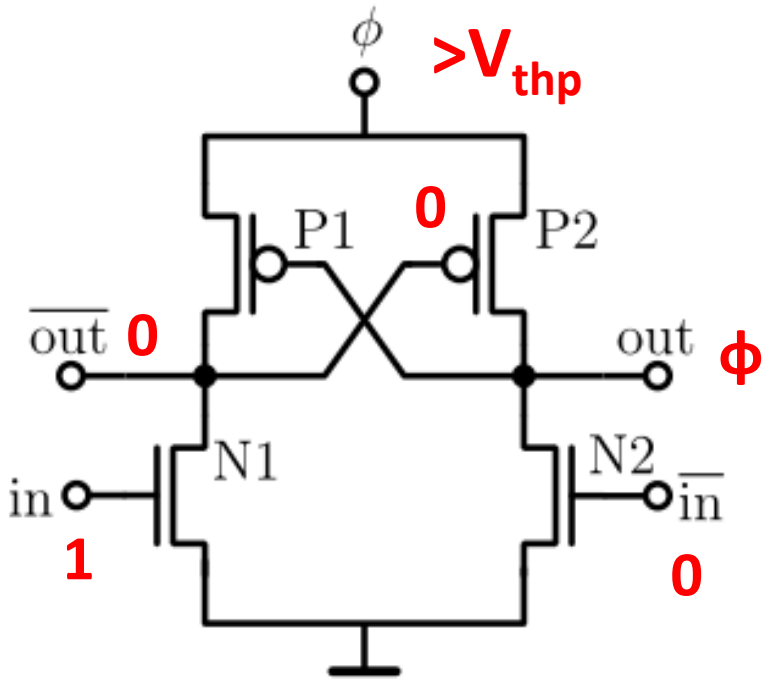
1-ECRL Buffer/Inverter (cont'd)



- Input signal is shifted by 90 degrees w.r.t to the power clock

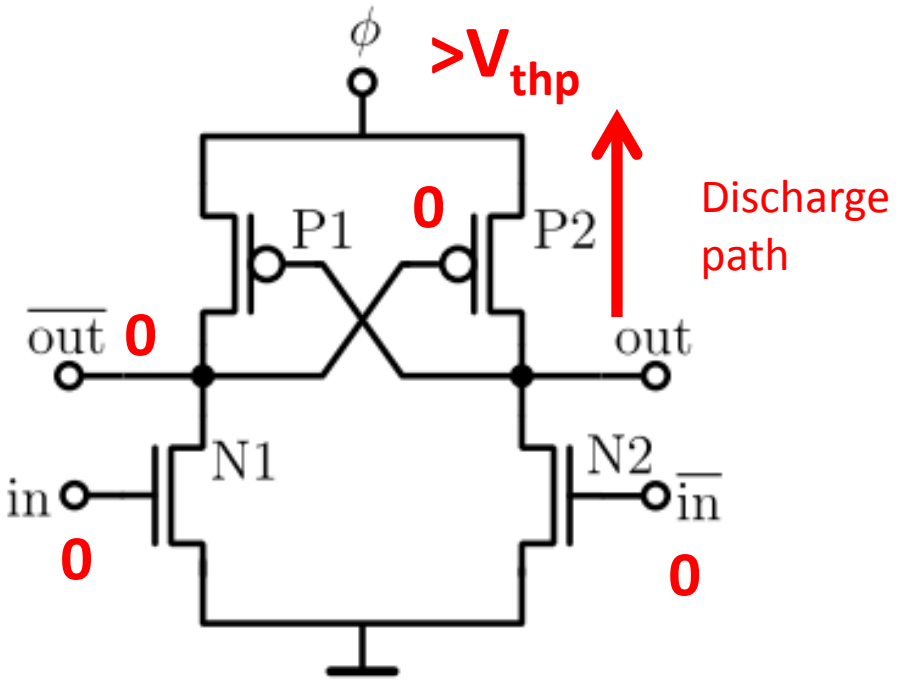
1-ECRL Buffer/Inverter (cont'd)

- Power clock ramping up from 0 to Vdd
- Out follows Power clock



1- ECRL Buffer/Inverter (cont'd)

- Power clock ramping down from Vdd to zero
- Both inputs are now zero
  - Because preceding stage is now recovering energy
  - Not strictly complementary
- N1 and N2 off



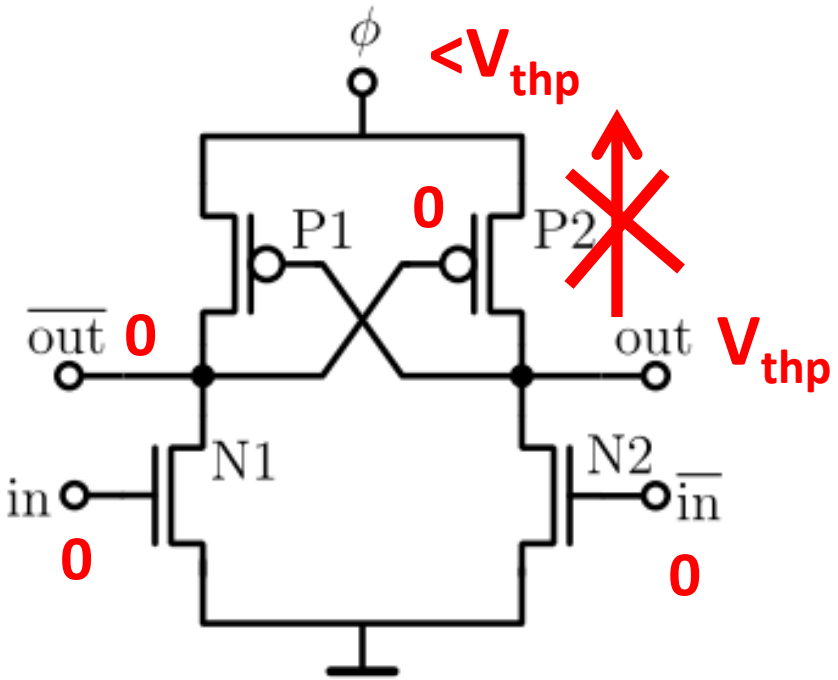
1- ECRL Buffer/Inverter (cont'd)

- $\Phi < V_{th,p}$
- Fraction of energy

  $= ½ C_{out} V^2_{th,p}$

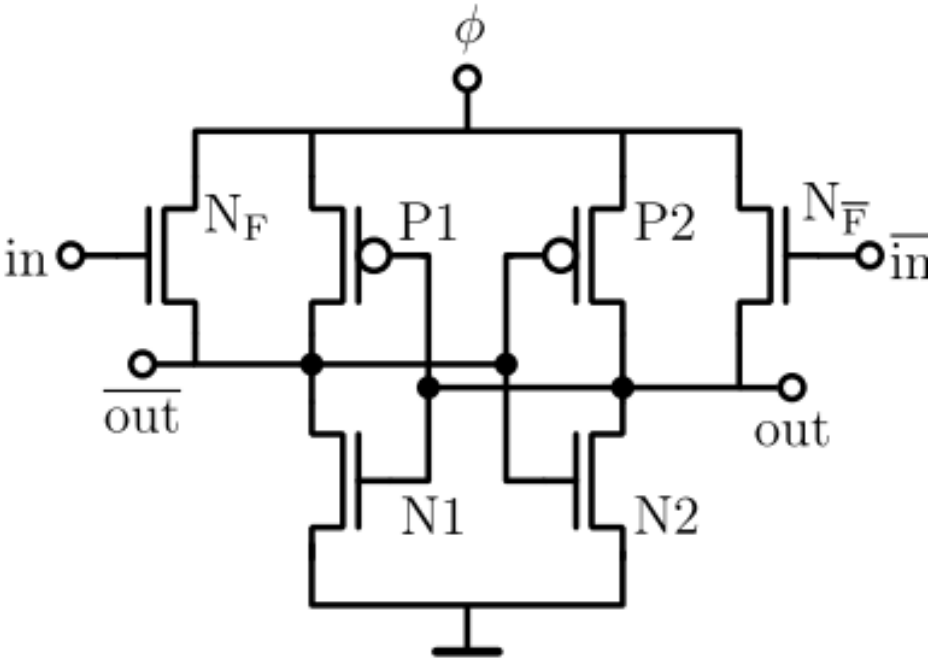
  dissipated or reused next cycle according to succeeding input signal

➔ Quasi-adiabatic



2-PFAL Inverter/buffer

- Consists of:
  - Latch made of 2 cross-coupled inverters
  - Logic function



ERCL vs PFAL

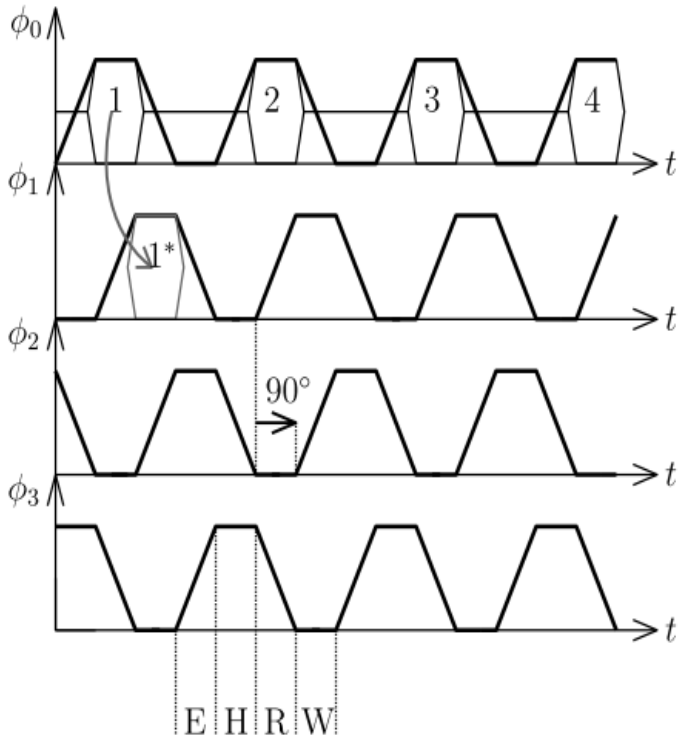
- ERCL: less number of transistors
- PFAL:
  - Functional block parallel to PMOS

  ➔less equivalent resistance

  ➔ less energy dissipated ($R^* C^2 * V_{dd}^2/T$)

4-Phase Power clock for Cascade

- **More than 1 power clock** used to operate **adiabatic system**
  - ERCL and PFAL use 4-phase power clock ϕ0-ϕ3
- Because input has to be stable in evaluation phase
  - ERCL and PFAL: 90° phase shift between subsequent phases is obtained



4-Phase Power clock for Cascade (cont'd)

- 4 – Phases:
  - *Evaluate (E)*: outputs are evaluated from stable input signals
  - *Hold (H):* outputs are kept stable to supply subsequent gate with stable input signal.
  - *Recover (R)*: Energy is recovered
  - *Wait (W)*: for symmetry reasons because symmetric signals are easier to generate

Power Supply

- LC circuit
- Stepwise charging
  - Charging of output to VDD is not done abruptly, but is divided into N steps

Cons and Pros

- Slower than conventional CMOS
- Requires special power supply
- Area (but we get function and its complement)
+ Less **Power** if high switching activity

  or disconnect system from power supply while idle (sleep transistors)

References

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