UCLA

Incremental Gate Sizing for Late Process Changes

John Lee and Puneet Gupta

UCLA

Late process changes?

- Aggressive schedules = uncertainty
  - From ITRS 2008:

Table DESN9 Design for Manufacturability Technology Requirements

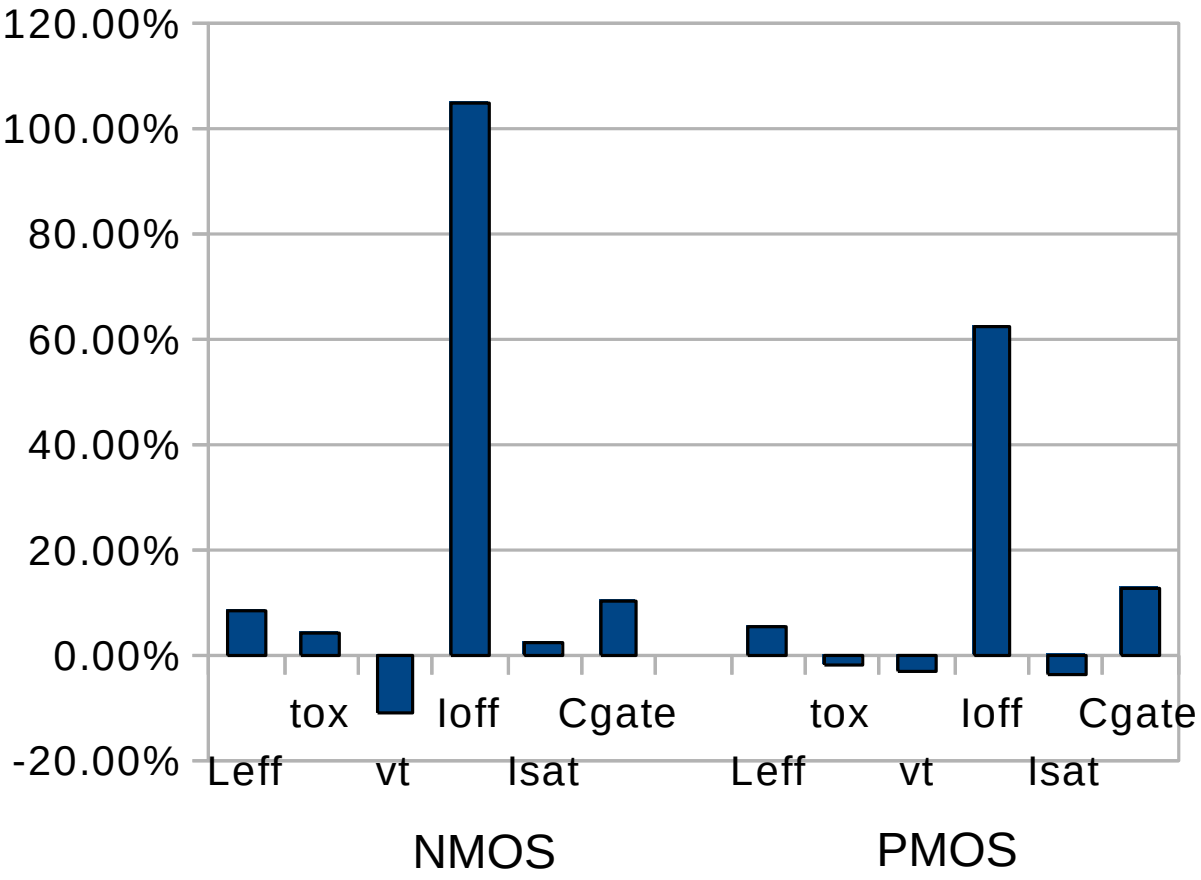
Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*
Normalized mask cost from public and IDM data	1	1.3	1.7	2.3	3	3.9
% V_{dd} variability: % variability seen in on-chip circuits	10%	10%	10%	10%	10%	10%
% V_{th} variability: doping variability impact on V_{th}, (minimum size devices, memory)	31%	35%	40%	40%	40%	58%
% V_{th} variability: includes all sources	33%	37%	42%	42%	42%	58%
% V_{th} variability: typical size logic devices, all sources	16%	18%	20%	20%	20%	26%
% CD variability	12%	12%	12%	12%	12%	12%
% circuit performance variability circuit comprising gates and wires	46%	48%	49%	51%	60%	63%
% circuit total power variability circuit comprising gates and wires	56%	57%	63%	68%	72%	76%
% circuit leakage power variability circuit comprising gates and wires	124%	143%	186%	229%	255%	281%

Solutions known, under development

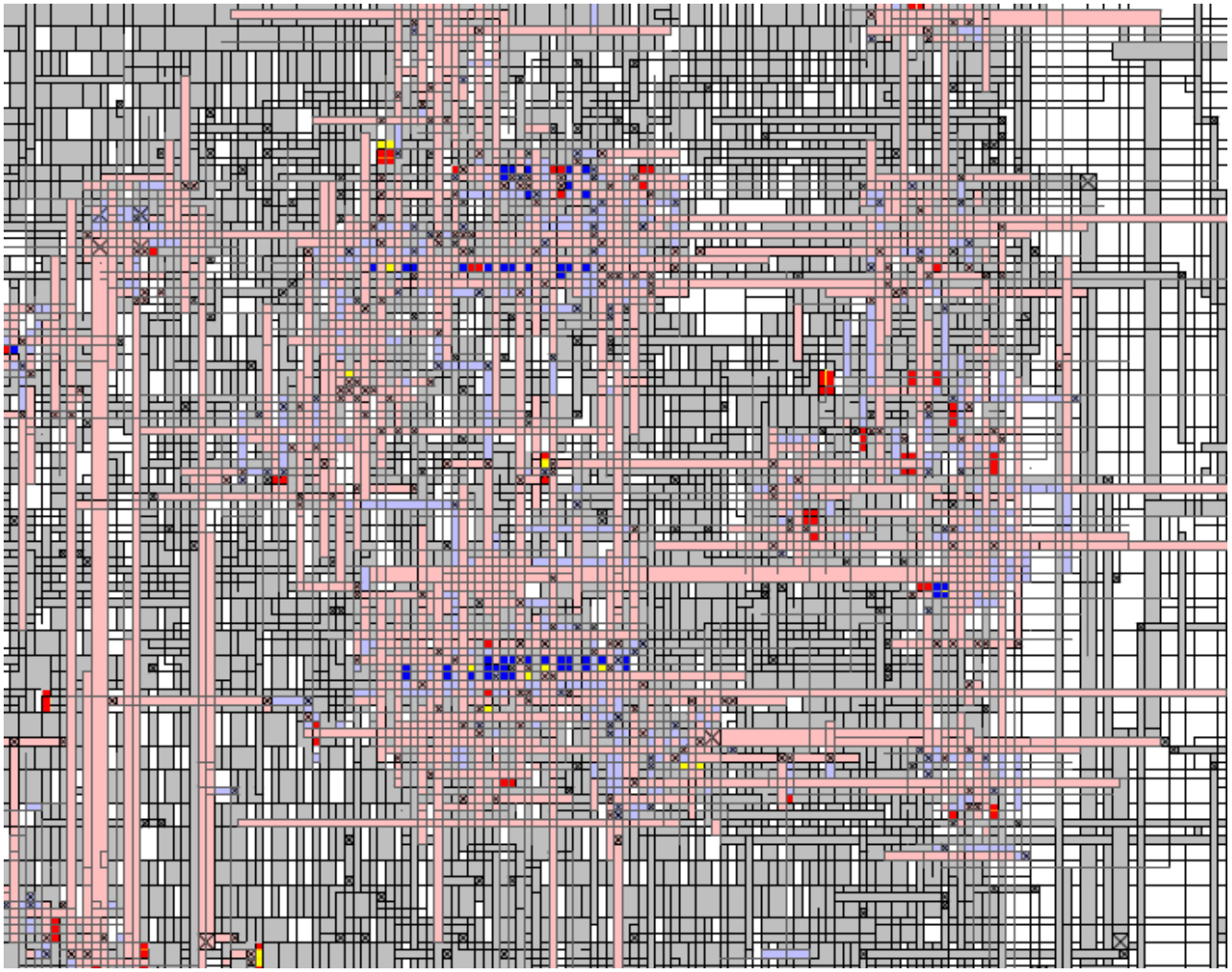
Solutions not known

45nm Process change example

- From April 2008 to March 2010



What does an ECO cost?



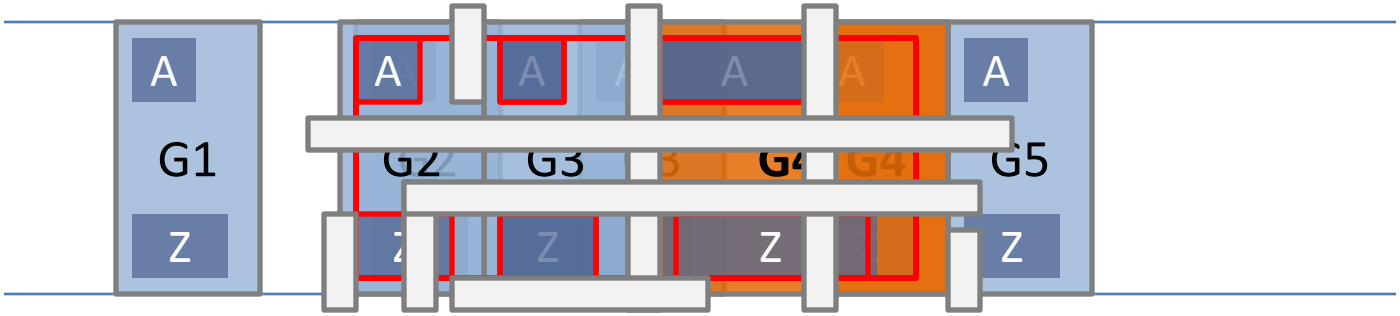
ECO Cost Measures

- **ECO Area Cost** – Changed area:
  - Amount of area that must be reanalyzed
    - Parasitic Extraction
    - LVS / DRC
  - Potential errors to be corrected

- **ECO Timing Cost** – Changed timing
  - The effect of the ECO on the timing signal
  - Changes flow downstream / upstream
  - Potential timing errors to be corrected

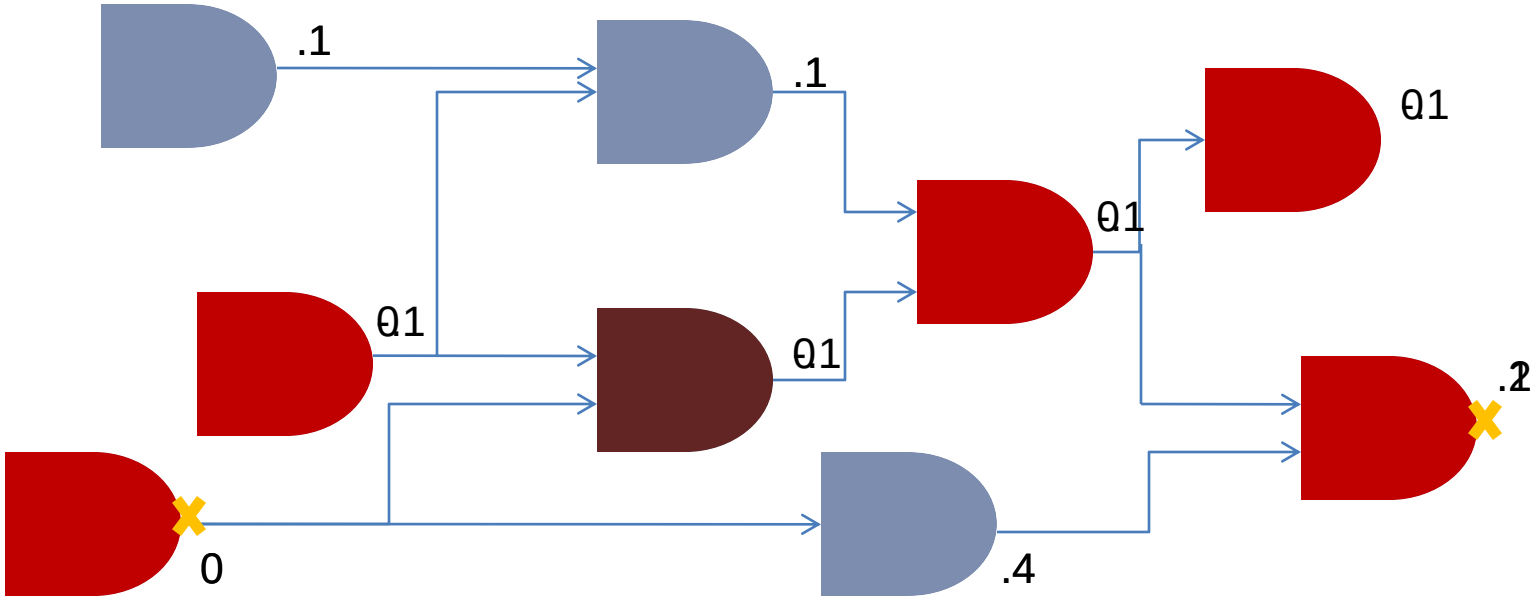
Modeling ECO Area Cost

- Eco Cost: amount of area, in μm^2 that has changed
  - Includes gate area, metal wires and vias
- Modeled as a linear function of:
  - Number of changed pins
  - Number dislocated pins
    - Old and new locations do not overlap
  - Area of the pin bounding box
  - Congestion over the pin bounding box



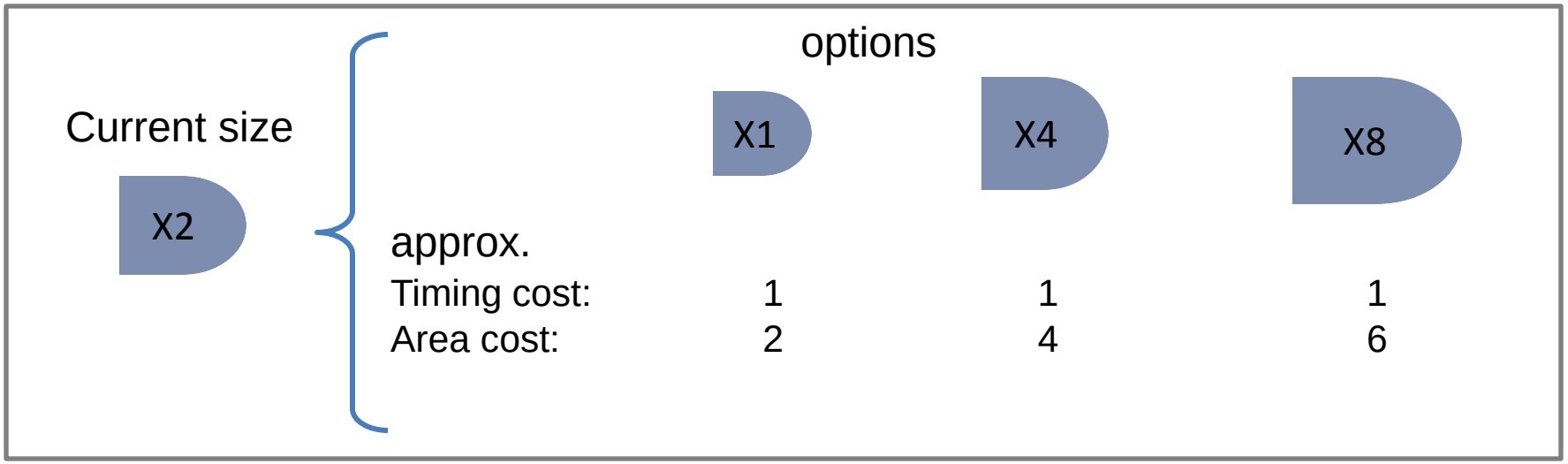
ECO Timing Cost

- Timing is affected downstream and upstream
- ECO Timing cost is defined as:
  - Number of non-critical pins that are upstream and downstream from an ECO



ECO-cost aware design via LPECO

- Linear programming based ECO gate sizing
  - Objective: ECO cost + Power cost
  - Constraints: Delay (timing closure)
- For timing **infeasible** problems:
  - Slack maximization

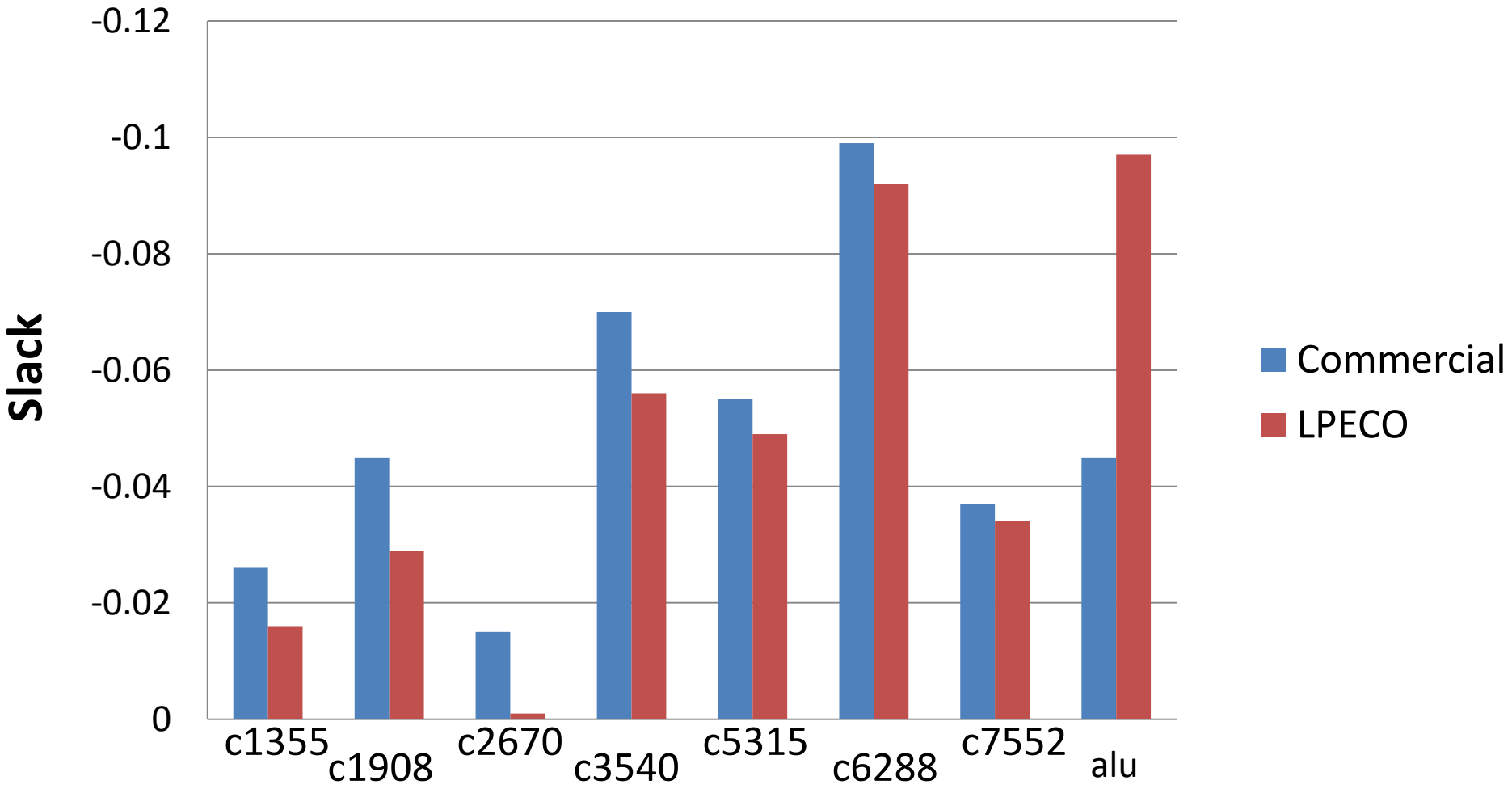


Experimental Setup

- 45nm Nangate Open Cell Library
- Manufacturing process change:

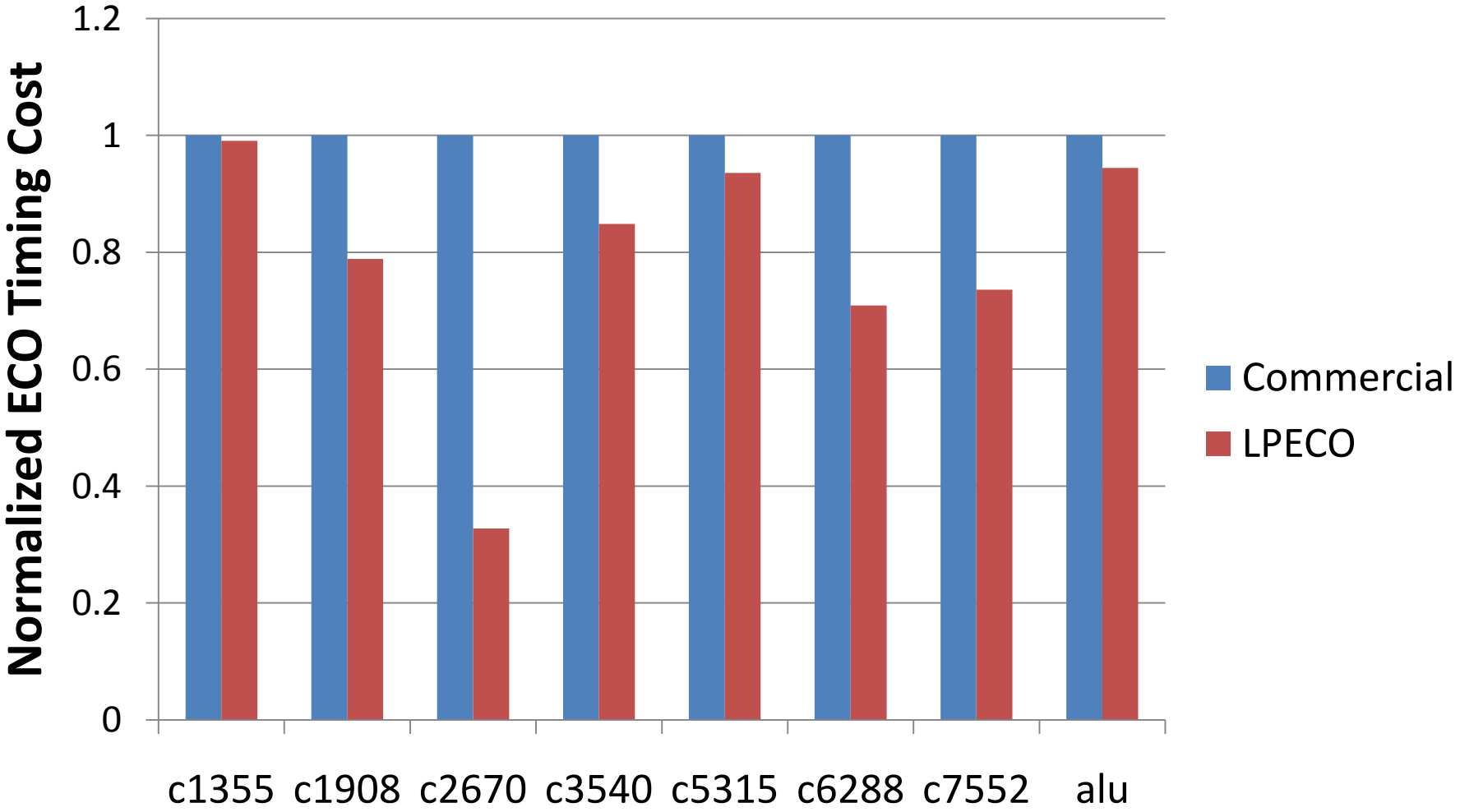
	Nmos		Pmos
Vt:	-10%	-5%	
tox:	+5%		-5%
cgate:	+10%	+10%	
leff:	+5%		+5%

Results: Slack maximization (infeasible designs)



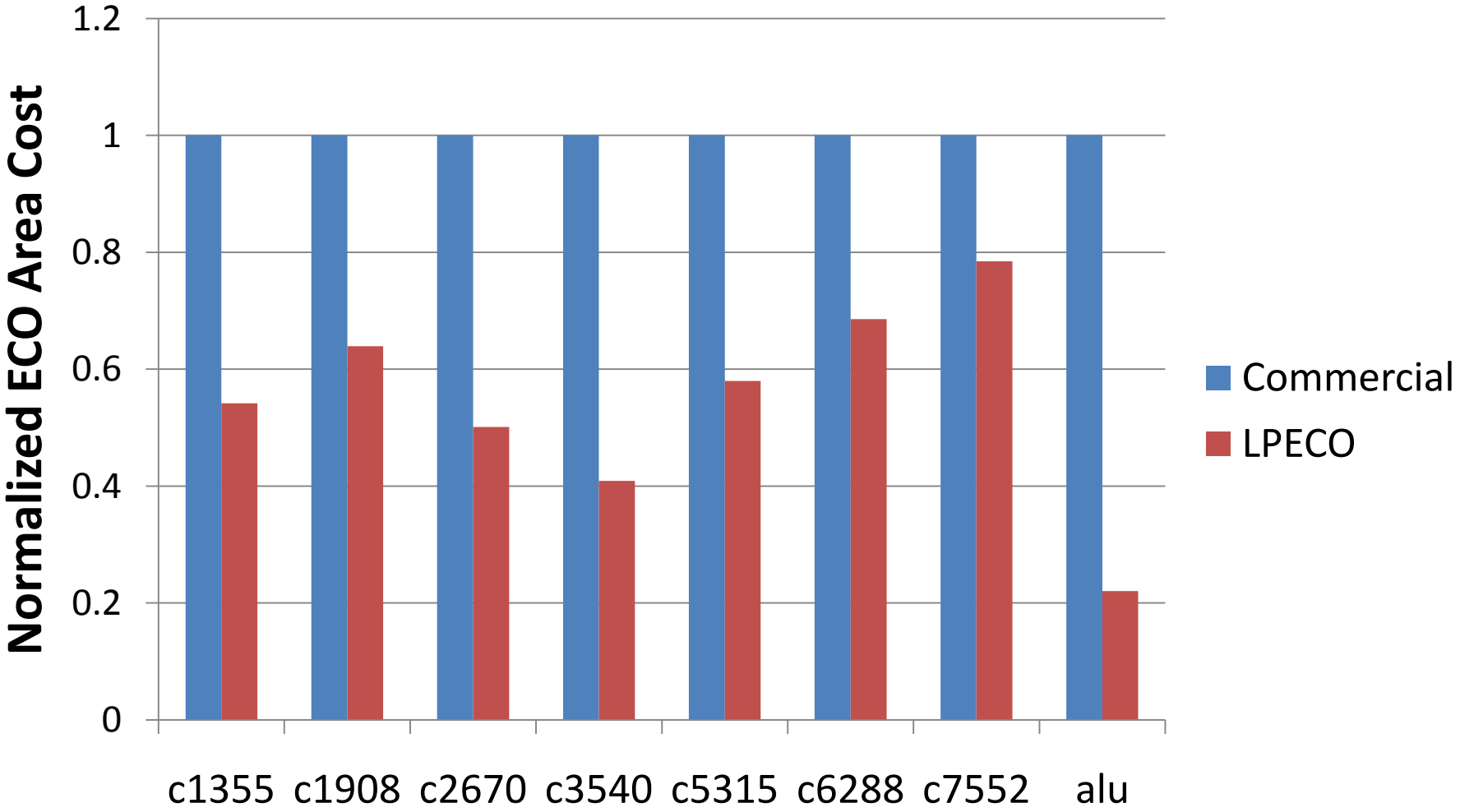
vt: nmos -10%, pmos -5%; tox: nmos +5%, pmos -5%;
cgate: nmos +10%, pmos +10%; leff: nmos +5%, pmos +5%

Results: Timing Cost Comparison



vt: nmos -10%, pmos -5%; tox: nmos +5%, pmos -5%;
cgate: nmos +10%, pmos +10%; leff: nmos +5%, pmos +5%

Results: Area Cost Comparison



vt: nmos -10%, pmos -5%; tox: nmos +5%, pmos -5%;
cgate: nmos +10%, pmos +10%; leff: nmos +5%, pmos +5%

Summary

- Quantified ECO Costs:
  - ECO Timing Cost
  - ECO Area Cost
- Performed incremental optimization to minimize ECO costs using LPECO
- Method performs well compared to commercial tool:
  - 22% to 88% reduction in ECO Area
  - 1% to 67% reduction in ECO Timing Cost
- Future goals:
  - Initial designs that incur small ECO penalties in the future
  - Large scale examples

Extra Slides

ECO-LP

$$
\begin{array}{ll}
\text{minimize} & \sum_{i,k} p_{ik} y_{ik} + \gamma \mathrm{ECO}(y; x) \\
\text{subject to} & t_i + d_{i0} + \sum_k \delta_{ik} y_{ik} \leq t_j, \quad \forall i \in \mathrm{fo}(j) \\
& t_i \leq T_{\max}, \quad \forall i \in \mathrm{po} \\
& \sum_k y_{ik} \leq 1, \quad \forall i \\
& \sum_k y_{ik} + \\
& \cdots \sum_{j \in \mathrm{fo}(i)} \sum_k y_{jk} + \sum_{j \in \mathrm{fi}(i)} \sum_k y_{jk} \leq 1, \quad \forall i \\
& 0 \leq y_{ik} \leq 1
\end{array}
\tag{2}
$$

The variables are:

- t_i: Arrival time for gate i
- d_{i0}: Current delay for gate i
- δ_{ik}: Change in the delay of gate i under size k
- y_{ik}: Assignment variable of gate i to size k
- p_{ik}: Power cost of changing gate i to size k