Intrusive Routing for Improved Standard Cell Pin Access

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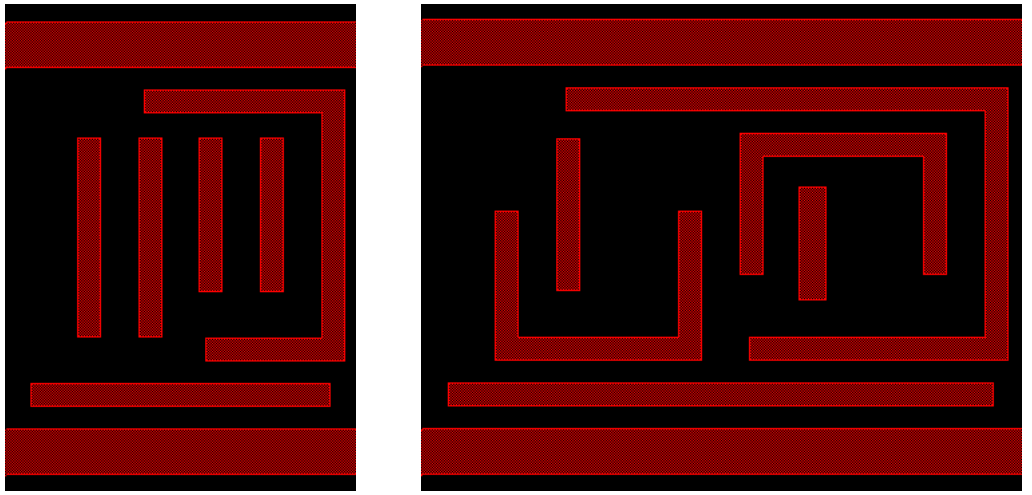
Motivation

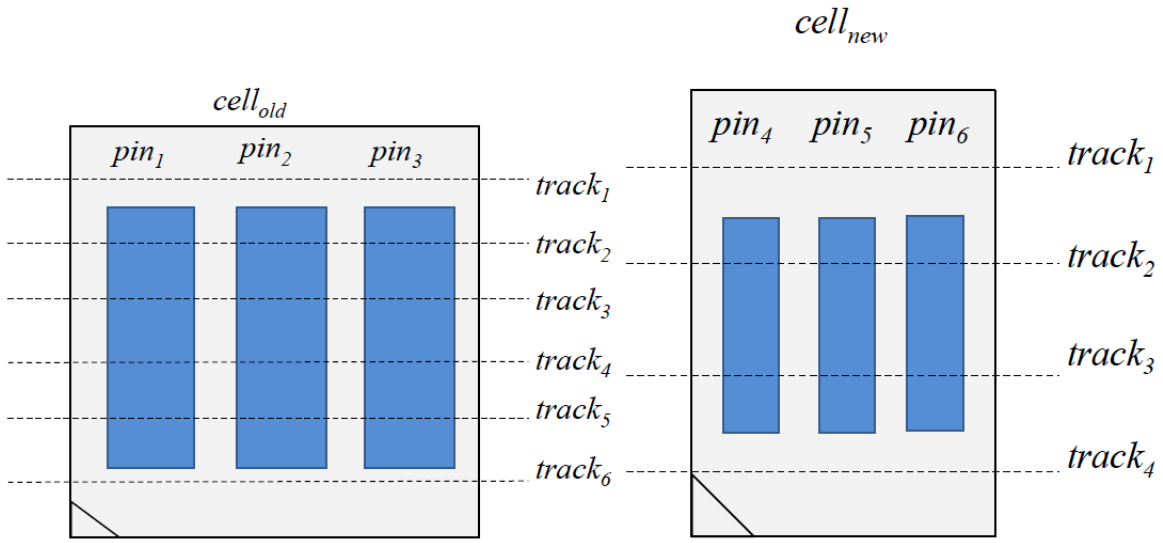
- Standard-cell Routability → critical physical design objective
  - Dictates area utilization, timing and signal integrity, DFM considerations

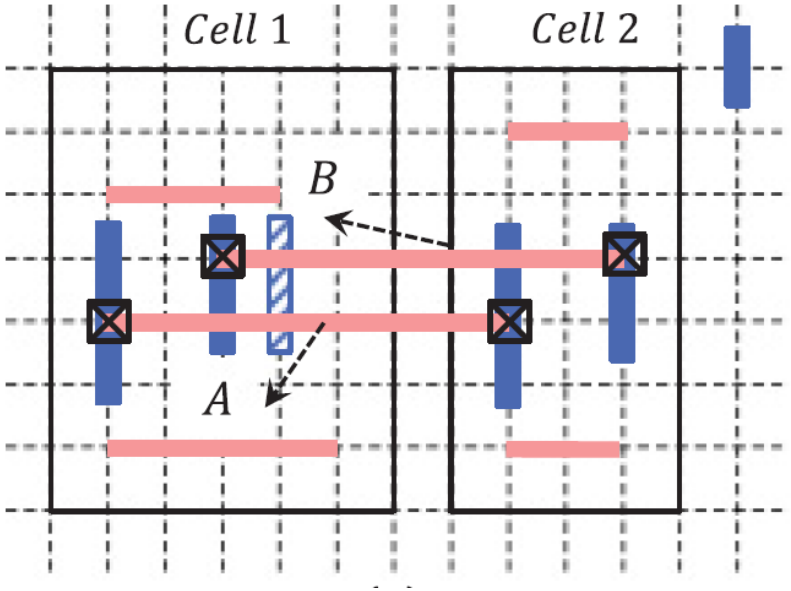
- Pin Access → key bottleneck
  - Device scaling → standard cell design complexity ↓, design rules ↑
  - Pin polygon size ↓ , #covering tracks ↓
  - Existing cell internal routing shapes → blockage in one or more directions
    - Larger design does not indicate better pin access

- Ideal internal routing configuration → still agnostic of true local congestion in placed cells



Pin Access Considerations





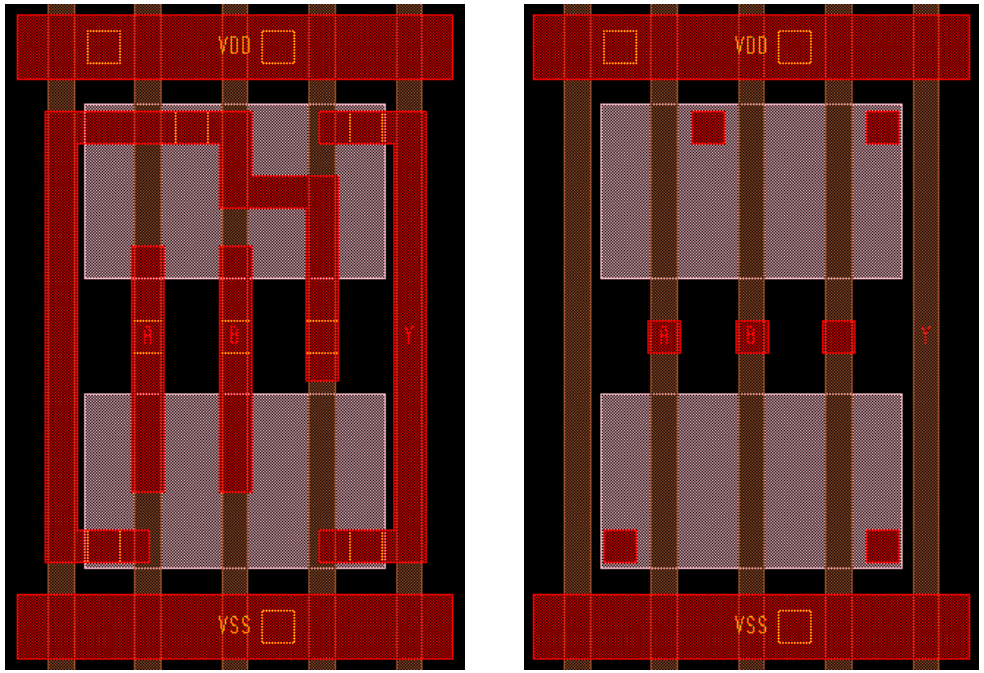
- Device scaling causes #tracks covering pin shape to decrease
- Existing nets might make a pin inaccessible due to track congestion

M-K. Hsu et al., "Design and manufacturing process co-optimization in nano-technology", *IEEE/ACM Int. Conf. Comp.-Aided Des. (ICCAD)*, pp. 574-581, Nov. 2014.

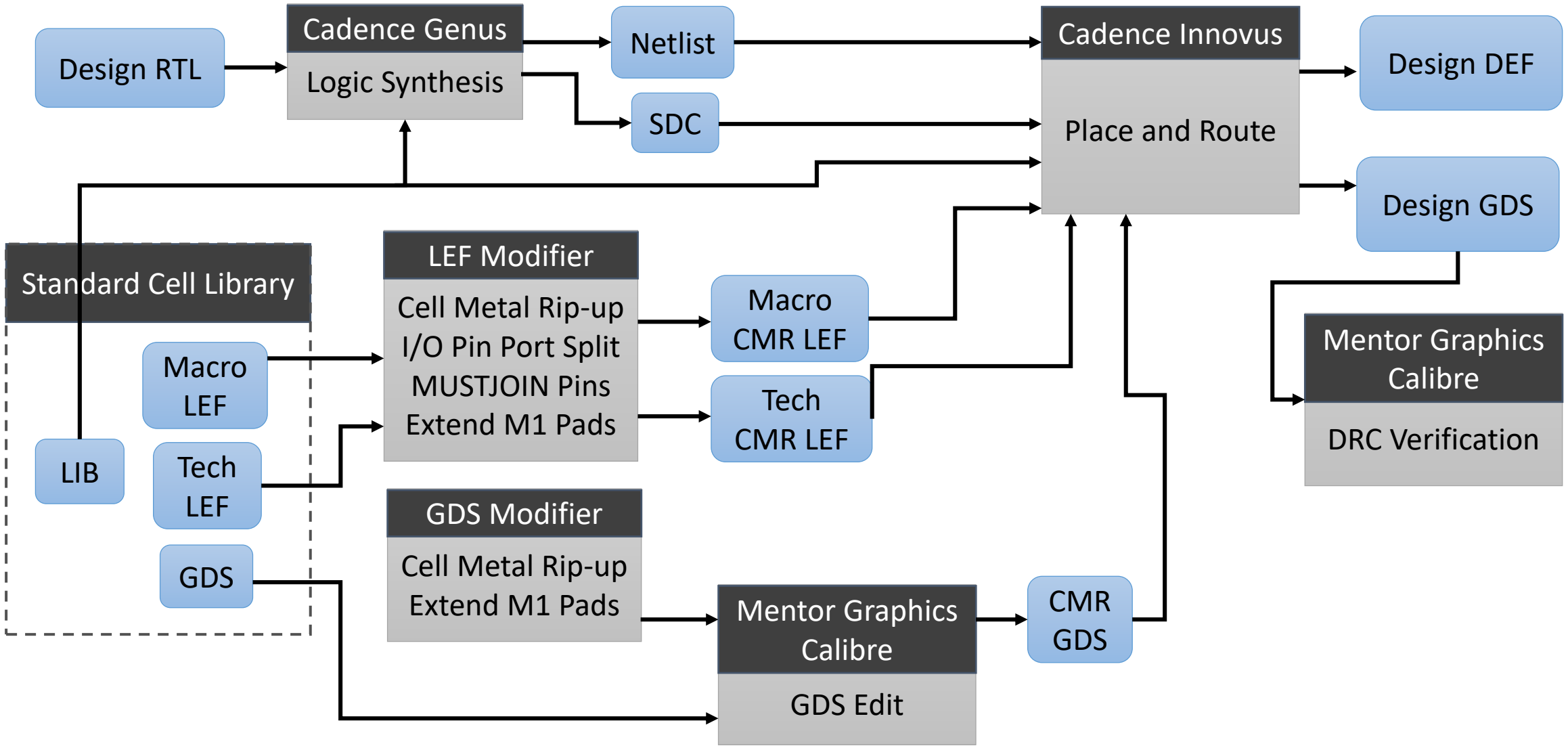
X. Xu, B. Yu, J-R. Gao, C-L. Hsu, and D. Z. Pan, "PARR: Pin-Access Planning and Regular Routing for Self-Aligned Double Patterning", *ACM Trans. Des. Automation of Electronic Syst. (TODAES)*, vol. 21, no. 3, Jul. 2016.

Approaches

- Complete intra-cell routing rip-up
  - Rip-up all internal metal layers, retain contacts, minimum-size M1 landing pads.
  - Communicate connectivity information to commercial router
    - Isolated I/O pin shapes
    - Internal nets
  - Near-optimal approach but inflated problem size
- Congestion-based selective intra-cell routing rip-up
  - Recognize areas with high congestion and/or routing violations
  - Selectively rip-up nets of specific std. cells
- Multiple cell pin-access configuration swap
  - Maintain multiple variants per cell based on pin access
  - Heuristically swap



Tool Flow Overview



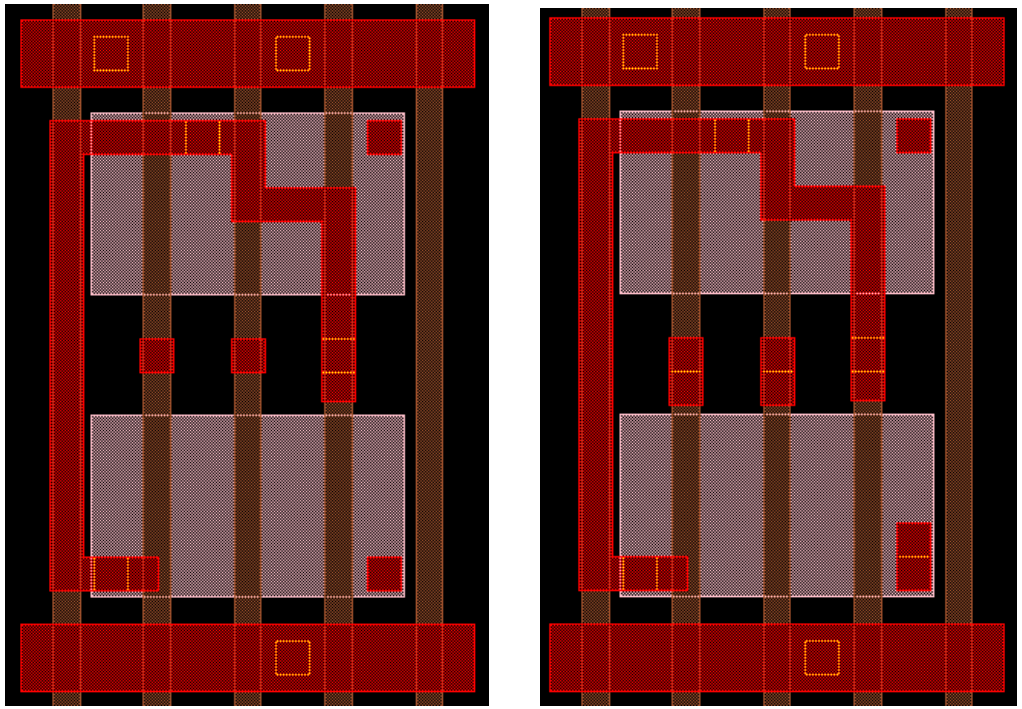
Library Modifications

- Primarily LEF and GDS edits for cell metal rip-up (CMR)
  - Pin-wise metal layer shapes available in LEF and GDS
  - Selectively parse and rip-up

- Communicating connectivity to the router:
  - Cell I/O signal shapes:
    - Split pin shapes into individual ports
    - LEF property: MUSTJOINALLPORTS
  - Cell internal nets – 3 options
    - MUSTJOIN pins – internal pins creating implicit nets for the router
    - Add new normal internal pins, normal nets to the DEF – comformity issue with netlist, Liberty
    - Virtual Pins – not supported

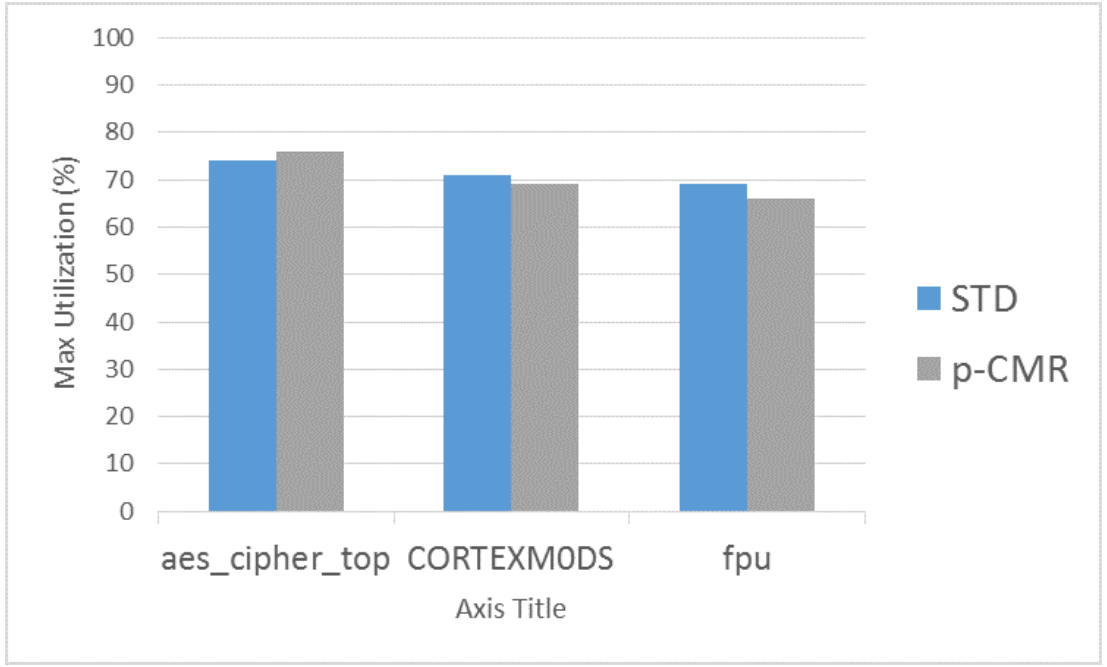
Experimental Setup

- Implemented basic version of proposed CMR approach for methodology validation
  - Partially rip-up internal nets of all cells – p-CMR
    - Rip-up all I/O pin shapes
    - Retain all original internal shapes
- Critical added constraint – track misalignment
  - Default M1 pads cover contacts – uneven spacing
- Extend M1 landing pads – atleast one M2 track should align
  - Simple approach – extend everything in one direction
  - If spacing violation, don't extend



Results

- Benchmarks from IWLS 2005 Benchmark Suite



- Heuristic utilization sweep to find minimum design area
  - Confidence interval of ±0.1%
- Routing-constrained designs – top routing layer chosen accordingly
- 50 DRC violation threshold

- Comparable utilization results.

EVALUATED BENCHMARK DESIGNS

Design	Size (#Gates)	Top Routing Layer
cortexm0ds	9k	M4
aes_cipher_top	14k	M4
fpu	33k	M3

Future Work

- Basic framework validated → extend to full implementation for real comparison

- Full CMR based on MUSTJOIN pins
  - Workaround for internal ‘floating net’ DRC violation
- Full CMR based on new DEF nets
  - Workaround for netlist/Liberty mismatch
- Smart M1 landing pad extensions
  - If spacing violation, extend in another direction
- Congestion/violation based CMR
  - Simple approach: find default routing violations, swap with CMR cell, retry
- Cell variant swapping
  - Different pin access configurations

Thank You!

References

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6. W. A. Dees, Jr. and P. G. Karger, ”Automated rip-up and reroute techniques”, *Des. Automation Conf. (DAC)*, pp. 432-439, 1982.
7. C. J. Alpert et al., ”What makes a design difficult to route”, *Int. Symp. Physical Design (ISPD)*, pp. 7-12, Mar. 2010.