

# Short Papers

## Efficient Additive Statistical Leakage Estimation

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**Abstract**—Nominal power estimation is quick but gives minimal information. Statistical power analysis can provide information on yield, chip robustness, etc., but current methods are unnecessarily slow and complex. This is primarily because existing leakage-power models, which model leakage power as lognormal distribution and calculate chip leakage power based on Wilkinson's approach, are not directly additive. Hence, for each incremental change of the circuit, the covariances between each pair of circuit elements need to be recalculated, which is inefficient. In this paper, we proposed a simple additive polynomial leakage-variation model. With additivity, we can calculate chip leakage power and leakage power after incremental change very efficiently. Experimental results show that our method is five times faster than the existing Wilkinson's approach while having no accuracy loss in mean estimation and about 1% accuracy loss in standard-deviation and 99%-percentile-point estimations.

**Index Terms**—Leakage power, process variation, yield modeling.

### I. INTRODUCTION

Nominal power analysis is and has been the standard way to estimate chip power. Although minimal information is obtained through this method (nominal chip power), it is both fast and incremental (requiring one simple addition per gate). On the other hand, statistical power analysis can provide the designer with a distribution of possible chip power consumption. This is very useful in estimating the parametric yield of a chip, thus directly translating into an estimation of profitability. Although this information is of great interest to chip manufacturers, there is currently no accurate statistical power modeling technique that is both fast and incremental. This makes statistical power analysis and optimization for large state-of-the-art chips a tedious task.

There have been many published approaches that cut dependence on full-circuit simulation altogether and are able to get decent results fairly fast [2]–[5]. Most of these works have been performed in regard to leakage power because it has the largest variance (it can vary 20 times while delay only changes 30%). These approaches still require complicated manipulation of their input parameters. Due to complex and interdependent parameter manipulation, these approaches are not incremental. Thus, even an  $\mathcal{O}\{N\}$  nonincremental algorithm would still be costly. Statistical power analysis through addition of distributions is another topic of research; however, these approaches all try to deal with the same snag. Leakage power is best characterized by a lognormal distribution; however, there is no closed-form solution to the addition of lognormals. Many of these approaches rely on Wilkinson's approach to lognormal addition. Although these ap-

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proaches find accurate solutions relatively quickly for smaller chips, any model that is primarily dependent on Wilkinson's approach ( $\mathcal{O}\{N^2\}$ ) will not be scalable to large chips. An excellent example of this type of approach can be found in [3]. Reference [4] seeks to extract low-ranking quadratic models for each gate and hierarchically combines them into a low-ranking quadratic model for the whole chip. Such a method is fast when computing full-chip leakage power; however, it cannot handle incremental changes efficiently.

There are some approaches that are incremental and linear [6]. Reference [6] tries to model leakage variation as a set of orthogonal polynomials. Such a method is incremental and time efficient. However, it requires a different set of orthogonal polynomials for different distributions of variation sources, which makes it not flexible for different types of variation sources.

As discussed previously, Wilkinson's approach, which most of the existing works are based on, is not directly additive. In order to calculate chip leakage power, the covariances of each pair of circuit elements need to be calculated. Moreover, during leakage-power optimization, some of the circuit elements of a chip may be incrementally changed. For Wilkinson's approach, the covariances between each pair of the changed circuit elements and the remaining circuit elements need to be recalculated, which is very inefficient. However, if we have a leakage-power model that is directly additive, we may greatly improve the efficiency of chip-leakage-power calculation and optimization. With additivity, we only need simple linear operations for both chip-leakage-power and incremental calculations.

To achieve the additivity goal, we express leakage power as a polynomial instead of an exponential function of variation sources so that it is additive. It is shown that, in order to recalculate the chip leakage variation after changing some circuit elements, the computational complexity of our approach does not depend on the number of circuit-element types (standard-cell-library size), while the complexity of Wilkinson's approach is linear to the circuit-element types.

The rest of this paper is organized as follows. Section II introduces the traditional Wilkinson's approach. Section III presents our additive leakage-variation model. Section IV further extends our model with the existence of within-die variation. Section V shows some experimental results, and finally, Section VI concludes this paper.

### II. WILKINSON'S APPROACH

Typically, leakage power is modeled as an exponential function of variation sources,  $P = P_0 \cdot e^{\sum c_i X_i}$ , where  $P_0$  is the nominal leakage value,  $X = (X_1, X_2, \dots, X_n)$  is the vector of variation sources, (e.g., effective channel length, threshold voltage, oxide thickness, etc.), and  $c_i$ 's are coefficients that can be obtained from curve fitting through SPICE simulation or measurement. In most cases, variation sources are assumed to be with Gaussian distribution. Therefore, cell leakage power is with lognormal distribution. With the single-cell leakage-power-variation model, full-chip leakage power is calculated as the sum of the leakage powers of all cells,  $P_{\text{chip}} = \sum_{i \in T} N_i P_i$ , where  $T$  is the set of all cell types in the chip,  $N_i$  is the number of the  $i$ th cell, and  $P_i$  is the leakage power of the  $i$ th cell. As discussed earlier,  $P_i$  is modeled as a lognormal random variable. Then,  $P_{\text{chip}}$  is the sum of lognormal random variables. However, there is no closed-form expression to calculate the distribution of the sum of lognormal distributions. The most popular method is to approximate the sum of

lognormal distributions as another lognormal distribution by matching the mean and variance, which is referred to as *Wilkinson's approach*,  $P_{\text{chip}} = \sum_{i \in T} N_i P_i \approx e^G$ ,  $\mu_G = \sum_{i \in T} N_i \mu_{P_i}$ , and  $\sigma_G^2 = \sum_{i \in T} N_i^2 \sigma_i^2 + \sum_{i,j \in T} N_i N_j \text{cov}_{P_{ij}}^2$ , where  $G$  is a Gaussian random variable with mean  $\mu_G$  and variance  $\sigma_G^2$ , and  $\mu_{P_i}$  and  $\sigma_{P_i}^2$  are the mean and variance of  $P_i$ , respectively. Wilkinson's approach provides a closed-form approximation of chip-leakage-power distribution. For Wilkinson's approach, in order to calculate full-chip leakage power, one needs to calculate the sum of covariances between each pair of circuit elements. Since there are  $N_t$  types of circuit elements in the circuit and, for each pair of circuit elements,  $n$  (number of variation sources) operations are required to calculate covariance, Wilkinson's approach's computational complexity is  $\mathcal{O}\{nN_t^2\}$ ,<sup>1</sup> where  $N_T = |T|$  is the number of circuit-element types (or the size of the standard cell library). However, Wilkinson's approach is not directly additive, i.e., if we change one type of circuit element, the full-chip mean and variance need to be recalculated. Therefore, it is not very efficient for full-chip-leakage-power optimization.

### III. ADDITIVE LEAKAGE-POWER MODEL

In this section, we introduce the additive leakage-power-variation model. The basic idea is to express leakage-power variation as a polynomial instead of an exponential function of variation sources, which is used in most of the statistical leakage analysis. Considering that leakage power is exponentially related to variation sources, in order to approximate leakage power accurately, we need high-order polynomials. In this paper, we approximate leakage power as a fourth-order polynomial of variation sources as follows:

$$P = P_0 \cdot \left( a_0 + \sum_{1 \leq i < j \leq n} (b_{ij1} X_i X_j + b_{ij2} X_i^2 X_j^2) + \sum_{1 \leq i \leq n} (a_{i1} X_i + a_{i2} X_i^2 + a_{i3} X_i^3 + a_{i4} X_i^4) \right) \quad (1)$$

where  $X = (X_1, X_2, \dots, X_n)$  is the vector of variation sources and  $a_{ik}$ ,  $b_{ijk}$ , and  $a_0$  are coefficients that can be obtained from curve fitting through SPICE simulation or measurement. In (1), we keep the first four order terms for each variation source and the first- and second-order pairwise crossing terms. There are  $n^2 + 3n + 1$  terms in total in the polynomial, where  $n$  is the number of variation sources. To achieve higher accuracy, users may use more terms at the cost of increased computational complexity.

With polynomial expression of leakage power, it is very easy to compute chip leakage power. Chip leakage power is calculated as the sum of the leakage powers of all circuit elements,  $P_{\text{chip}} = \sum_{i \in T} N_i P_i$ , where  $T$  is the set of element types of the circuit and  $N_i$  is the number of circuit elements of type  $i$ . Since the leakage powers of all circuit elements are expressed in a polynomial form as in (1), it is easy to see that  $P_{\text{chip}}$  is also in the same form. However, we still need to obtain the distribution of chip leakage power. We approximate chip leakage as a lognormal random variable by matching the mean and variance [7]. That is  $P \approx P_0 e^{R_N}$ , where  $R_N$  is a Gaussian random variable. Without loss of generality, assume that all variation sources

are with zero mean and unit variance. From (1), it is easy to find that the mean of leakage power can be calculated as

$$\begin{aligned} \mu_P &= E[P] \\ &= P_0 \left( a_0 + \sum_{1 \leq i < j \leq n} b_{ij2} + \sum_{1 \leq i \leq n} (a_{i2} + a_{i3} m_{i3} + a_{i4} m_{i4}) \right) \end{aligned} \quad (2)$$

$$\begin{aligned} m_{2P} &= E[P^2] \\ &= P_0 \left( a_0^2 + \sum_{1 \leq i \leq n} (2a_0 a_{i2} + 2a_0 a_{i3} m_{i3} + 2a_0 a_{i4} m_{i4} \right. \\ &\quad + a_{i1}^2 + a_{i2}^2 m_{i4} + a_{i3}^2 m_{i6} \\ &\quad + a_{i4}^2 m_{i8} + 2a_{i1} a_{i2} m_{i3} \\ &\quad + 2a_{i1} a_{i3} m_{i4} + 2a_{i1} a_{i4} m_{i5} \\ &\quad + 2a_{i2} a_{i3} m_{i5} + 2a_{i2} a_{i4} m_{i6} \\ &\quad + 2a_{i3} a_{i4} m_{i7}) \\ &\quad + \sum_{1 \leq i < j \leq n} (2a_0 b_{ij2} + b_{ij1}^2 + b_{ij2}^2 m_{i4} m_{j4} \\ &\quad + 2b_{ij1} b_{ij2} m_{i3} m_{j3} + 2a_{i2} a_{j2} \\ &\quad + 2a_{i2} a_{j3} m_{i2} m_{j3} \\ &\quad + 2a_{i2} a_{j4} m_{i2} m_{j4} \\ &\quad + 2a_{i3} a_{j4} m_{i3} m_{j4}) \left. \right) \end{aligned} \quad (3)$$

$$\sigma_P^2 = m_{2P} - \mu_P^2 \quad (4)$$

where  $m_{ik}$  is the  $k$ th-order moment for the  $i$ th variation source  $X_i$ . After obtaining the mean and variance of  $P$ , we may obtain the mean and variance of  $R_N$  in the same way as [7],  $\mu_N = 2 \log \mu_P - 0.5 \log(\mu_P^2 + \sigma_P^2) - \log P_0$  and  $\sigma_N = \log(\mu_P^2 + \sigma_P^2) - 2 \log(\mu_P)$ . With the aforementioned approximation, we may obtain the statistical characteristics of chip leakage power. For example, the  $Y\%$  percentile point  $W$  can be calculated as  $W = \sqrt{2} \sigma_N \text{erf}^{-1}(2Y - 1) + \mu_N$ .

From the previous discussion, we see that, in order to compute the chip-leakage-power variation, we need to calculate the sum of  $N_t$  polynomials with  $K$  terms. Moreover, we also need to calculate the square of a  $K$ -term polynomial. Therefore, the total computational complexity is  $\mathcal{O}\{KN_t + K^2\}$ . As discussed before, in this paper, we assume that  $K = n^2 + 3n + 1$ , which is the number of terms in (1). In practice, users may choose a different number of terms for the polynomial model. There is tradeoff between efficiency and accuracy. For example, we may approximate cell leakage power in a simpler or more complicated polynomial model as follows:

$$P = P_0 \cdot \left( a_0 + \sum_{1 \leq i < j \leq n} (b_{ij1} X_i X_j) + \sum_{1 \leq i \leq n} (a_{i1} X_i + a_{i2} X_i^2 + a_{i3} X_i^3) \right) \quad (5)$$

$$\begin{aligned} P &= P_0 \cdot \left( a_0 + \sum_{1 \leq i < j \leq n} (b_{ij1} X_i X_j + b_{ij2} X_i^2 X_j^2 + b_{ij3} X_i^3 X_j^3 \right. \\ &\quad + b_{ij4} X_i^2 X_j b_{ij5} X_i X_j^2) \\ &\quad + \sum_{1 \leq i \leq n} (a_{i1} X_i + a_{i2} X_i^2 + a_{i3} X_i^3 + a_{i4} X_i^4 + a_{i5} X_i^5) \left. \right) \end{aligned} \quad (6)$$

<sup>1</sup>Here, we assume that all covariance terms are calculated and stored in a lookup table. Otherwise, the computational complexity of Wilkinson's approach is even higher.

TABLE I  
LEAKAGE ERROR PERCENTAGE WITH RANGING NUMBERS OF POLYNOMIAL TERMS

bench mark	Wilkinson (%)				Equation (12) (%)					Equation (4) (%)					Equation (13) (%)				
	$\mu$	$\sigma$	99%	$T$ (ms)	$K$	$\mu$	$\sigma$	99%	$T$ (ms)	$K$	$\mu$	$\sigma$	99%	$T$ (ms)	$K$	$\mu$	$\sigma$	99%	$T$ (ms)
c1355	-0.3	-1.2	-1.7	860	7	-0.4	-5.8	-5.2	94	11	+0.2	-3.0	-3.1	133	16	-0.3	-2.4	-2.7	188
c1908	+0.1	-3.3	-1.1	842	7	-0.7	-5.9	-4.9	91	11	-0.1	-2.5	-0.7	131	16	-0.2	-2.4	-0.6	165
c3540	-0.5	-1.2	-3.5	912	7	-0.6	-4.8	-5.3	114	11	-1.3	-2.7	-3.4	154	16	-1.0	-1.9	-3.0	232
c5315	+0.1	-3.4	-0.6	930	7	-0.3	-6.4	-4.9	123	11	-0.0	-4.0	-1.8	1591	16	-0.0	-3.2	-1.4	258
c6288	-0.2	-1.9	-0.7	893	7	-0.3	-5.2	-7.1	109	11	-0.3	-3.5	-2.2	139	16	-0.2	-2.7	-1.2	226
c7552	-0.2	-1.6	-1.2	895	7	-0.7	-9.8	-8.2	114	11	-0.2	-5.2	-2.1	153	16	-0.2	-1.9	-1.3	238
ave	0.2	1.9	1.4	888	7	0.5	6.2	5.9	124	11	0.4	3.4	2.1	145	16	0.3	2.3	1.6	215

Equation (5) illustrates a simpler polynomial model that has only  $n(n-1)/2 + 3n + 1$  terms, while (6) illustrates a more complicated polynomial model that has  $5n(n-1)/2 + 5n + 1$  terms. Table I compares the error percentage of mean, variance, and 99% percentile point for the model in (1), (5), and (6). In the table, the average error percentage is calculated as the average of the absolute value. From the table, we find that accuracy increases as the number of polynomial terms increases, as expected. However, when the number of polynomial terms increases to a certain value as in the model of (6), the improvement of accuracy is limited. Therefore, in this paper, we will apply the model in (1).

On the other hand, the computational complexity for Wilkinson's approach is  $N_t^2$ , as discussed in Section II. Since the number of polynomial terms  $K$  is usually much smaller than the number of element types  $N_t$ , our method will be more efficient than Wilkinson's approach.

Moreover, during circuit optimization, fast incremental evaluation of power due to small circuit change is necessary. For Wilkinson's approach, if one of the circuit elements is changed in the circuit, the sum of covariances between the changed circuit element and the remaining circuit elements needs to be recalculated; therefore, the computational complexity of recalculating chip leakage is  $\mathcal{O}\{N_t\}$ . However, for our method, we only need to calculate the sum of two  $\mathcal{O}\{K\}$  polynomials and recalculate the mean and variance. In order to calculate the variance of a  $K$ -term polynomial, we need to calculate the mean of the square of it, which has  $K^2$  terms. Therefore, the computational complexity of recalculating chip leakage is  $\mathcal{O}\{K^2\}$ . That is, to recalculate chip leakage power, the computational complexity of our method does not depend on the number of circuit-element types (size of the standard cell library).

To show the efficiency of our approach, let us observe a simple example. Assume that we are going to calculate the leakage power of a circuit with 100 types of different circuit elements with two variation sources. For Wilkinson's approach, it needs to calculate the sum of the covariances of each pair of types. There will be  $100 \times (100 - 1)/2 = 4950$  pairs in total. However, for our approach, it only needs to calculate the sum of 100 polynomials with 11 terms. Moreover, if we want to incrementally calculate chip leakage power when one circuit element is changed, for Wilkinson's approach, the sum of covariances between this circuit element and all other circuit elements needs to be calculated, and there will be 99 covariances. However, for our approach, we only need to calculate the sum of two 11-term polynomials.

#### IV. HANDLING WITHIN-DIE VARIATION

In the previous section, we have introduced an additive polynomial leakage-power-variation model. Such a model works well when there is only interdie variation. In this section, we further discuss how to handle within-die variation in our model.

In practice, process variation is decomposed into interdie, within-die spatial, and within-die random variations  $X = X_g + X_s + X_r$ , where  $X_g$  is the interdie variation,  $X_s$  is the within-die spatial variation, and  $X_r$  is the within-die random variation. Considering the within-die

variation, the polynomial term  $X^k$  in (1) becomes  $(X_g + X_s + X_r)^k$ . Because  $X_s$  and  $X_r$  are different for different cells, such terms are not directly additive. In this case, we need to simplify the model to make it additive. First, we consider the within-die random variation. The polynomial term  $X^k$  can be calculated as

$$X^k = (X_g + X_s + X_r)^k = \sum_{i=1}^k \binom{k}{i} (X_g + X_s)^{k-i} X_r^i. \quad (7)$$

In practice, there are many cells of the same type with the same  $X_s$  and  $X_g$ . Therefore, we need to compute the sum of the leakage powers of a large number of cells of the same type, and the  $X_r$ 's for different cells are independent. Therefore, due to the central limit theorem, similar to the method in [1], we may approximate the aforesaid equation as

$$X^k \approx \sum_{i=1}^k \binom{k}{i} (X_g + X_s)^{k-i} E[X_r^i] \quad (8)$$

where  $E[X_r^i]$  can be obtained by the distribution of  $X_r$ . In this case, within-die variation is modeled as the change of polynomial coefficients.

Second, let us consider spatial variation. Because  $X_s$ 's are correlated for different cells, we cannot apply the central limit theorem on it. In this case, we apply the grid-based spatial-variation model. That is, a chip is divided into several grids, and all cells within the same grid have the same spatial variation. The spatial variation of different grids is correlated. Moreover, by applying principal component analysis (PCA) on spatial variation, spatial variation can be expressed as a linear combination of principal components

$$X_s = \sum p_i X_{pi}.$$

Then, the terms  $(X_g + X_s)^k = (X_g + \sum p_i X_{pi})^k$ . We may regard  $X_{pi}$ 's and  $X_g$ 's as different variation sources and then obtain the polynomial expression by expanding  $(X_g + \sum p_i X_{pi})^k$ . One problem is that expanding  $(X_g + \sum p_i X_{pi})^k$  results to a lot of terms and makes the polynomial very complex. However, considering the fact that spatial variation is usually not significant [8], [9], we may ignore the crossing terms of spatial variation without loss of much accuracy. Therefore, in the expansion, we may only keep the first three order terms of spatial variation and the first-order crossing terms between spatial variation and the corresponding interdie variation

$$\begin{aligned} (X_g + \sum p_i X_{pi})^k &\approx X_g^k + X_g^{k-1} X_{pi} + X_g^{k-2} X_{pi}^2 + X_g^{k-3} X_{pi}^3 \\ &+ \sum_{1 \leq i \leq g_s} (X_{pi} + X_{pi}^2 + X_{pi}^3 + k X_{pi} X_g) \end{aligned} \quad (9)$$

where  $g_s$  is the number of grids (number of spatial-variation sources). With such approximation, in the polynomial expression of leakage power, we have  $n^2 + 3n + 1$  terms for interdie variation, as discussed in the previous section, and for each variation source, we have  $4g_s$  terms for within-die spatial variation and  $2g_s$  terms for the crossing terms between spatial and interdie variations. Therefore, the total

TABLE II  
MEAN, STANDARD-DEVIATION, AND 99%-PERCENTILE-POINT COMPARISON FOR FULL-CHIP LEAKAGE POWER FOR FPGA BENCHMARKS

Bench mark	$N_t$	Our Method				Wilkinson				MC		
		$\mu$ (mW)	$\sigma$ (mW)	99% (mW)	T (ms)	$\mu$ (mW)	$\sigma$ (mW)	99% (mW)	T (ms)	$\mu$ (mW)	$\sigma$ (mW)	99% (mW)
alu4	17	16.2 (+0.0%)	8.5 (-4.5%)	30.4 (-3.2%)	67 (4.8X)	16.1 (-0.6%)	8.7 (-2.2%)	30.9 (-1.5%)	321	16.2	8.9	31.4
clma	17	98.1 (-0.2%)	53.4 (-3.0%)	224.1 (-1.9%)	66 (4.9X)	97.9 (-0.4%)	54.8 (-0.6%)	225.2 (-1.4%)	321	98.3	55.1	228.5
des	17	24.4 (-0.8%)	10.7 (-3.6%)	49.8 (-2.1%)	66 (4.9X)	24.5 (-0.4%)	10.8 (-2.7%)	50.1 (-1.5%)	321	24.6	11.1	50.9
deffeq	17	24.4 (+0.1%)	10.8 (-5.3%)	48.6 (-1.2%)	67 (4.6X)	24.3 (-0.4%)	11.0 (-3.5%)	48.9 (-0.6%)	320	24.4	11.4	49.2
dsip	17	20.4 (-0.1%)	10.4 (-2.0%)	34.2 (-3.7%)	66 (4.7X)	20.3 (-0.5%)	10.3 (-2.9%)	35.1 (-1.1%)	320	20.4	10.6	35.5
ave	-	0.3%	3.5%	2.2%	66 (4.8X)	0.4%	2.1%	1.3%	320	-	-	-

TABLE III  
MEAN, STANDARD-DEVIATION, AND 99%-PERCENTILE-POINT COMPARISON FOR INCREMENTAL LEAKAGE-POWER CALCULATION FOR FPGA BENCHMARKS

Bench mark	$N_t$	Our Method				Wilkinson				MC		
		$\mu$ (mW)	$\sigma$ (mW)	99% (mW)	T (ms)	$\mu$ (mW)	$\sigma$ (mW)	99% (mW)	T (ms)	$\mu$ (mW)	$\sigma$ (mW)	99% (mW)
alu4	17	16.9 (-0.6%)	8.8 (-2.1%)	32.2 (-2.8%)	15 (5.5X)	16.8 (-1.2%)	9.0 (-1.1%)	32.4 (-2.3%)	82	17.0	9.1	33.1
clma	17	98.9 (-0.2%)	54.7 (-2.8%)	227.1 (-1.3%)	16 (5.1X)	98.9 (-0.2%)	55.9 (-0.6%)	228.3 (-0.8%)	82	99.1	56.2	230.4
des	17	26.6 (-0.4%)	11.3 (5.0%)	51.6 (-2.5%)	16 (5.1X)	26.5 (-0.8%)	11.2 (5.9%)	52.1 (-1.6%)	82	26.7	11.9	52.9
deffeq	17	26.7 (+0.1%)	11.2 (-7.4%)	50.3 (-4.4%)	15 (5.4X)	26.7 (-0.1%)	11.6 (-4.1%)	51.1 (-2.9%)	81	26.7	12.1	52.6
dsip	17	21.7 (-0.1%)	11.5 (-6.6%)	35.3 (-3.7%)	15 (4.7X)	21.6 (-0.5%)	11.7 (-4.9%)	35.8 (-1.1%)	82	21.7	12.3	36.8
ave	-	0.3%	4.0%	2.6%	15 (5.5X)	0.5%	2.9%	1.5%	82	-	-	-

TABLE IV  
MEAN, STANDARD-DEVIATION, AND 99%-PERCENTILE-POINT COMPARISON FOR FULL-CHIP CALCULATION OF LEAKAGE POWER FOR ISCAS85 STANDARD CELL BENCHMARKS

Bench mark	$N_t$	Our Method				Wilkinson				MC		
		$\mu$ (mW)	$\sigma$ (mW)	99% (mW)	T (ms)	$\mu$ (mW)	$\sigma$ (mW)	99% (mW)	T (ms)	$\mu$ (mW)	$\sigma$ (mW)	99% (mW)
c1355	39	6.67 (+0.2%)	1.62 (-3.0%)	10.12 (-3.1%)	133 (6.5X)	6.68 (-0.3%)	1.65 (-1.2%)	10.36 (-1.7%)	860	6.66	1.67	10.54
c1908	32	9.92 (-0.1%)	2.06 (-2.5%)	15.14 (-0.7%)	131 (6.4X)	9.94 (+0.1%)	2.04 (-3.3%)	15.07 (-1.1%)	842	9.93	2.11	15.24
c3540	46	20.23 (-1.3%)	3.96 (-2.7%)	28.35 (-3.4%)	154 (5.9X)	20.38 (-0.5%)	4.02 (-1.2%)	28.34 (-3.5%)	912	20.49	4.07	29.36
c6288	43	30.36 (-0.3%)	6.68 (-3.5%)	43.25 (-2.2%)	139 (6.4X)	30.39 (-0.2%)	6.79 (-1.9%)	43.86 (-0.7%)	893	30.45	6.92	44.15
c7552	45	45.68 (-0.2%)	10.32 (-5.2%)	67.68 (-2.1%)	153 (5.8X)	45.69 (-0.2%)	10.68 (-1.6%)	68.42 (-1.2%)	895	45.78	10.85	69.21
ave	-	0.4%	3.4%	2.1%	145 (6.1X)	0.2%	1.9%	1.4%	888	-	-	-

TABLE V  
MEAN, STANDARD-DEVIATION, AND 99%-PERCENTILE-POINT COMPARISON FOR INCREMENTAL CALCULATION OF LEAKAGE POWER FOR ISCAS85 STANDARD CELL BENCHMARKS

Bench mark	$N_t$	Our Method				Wilkinson				MC		
		$\mu$ (mW)	$\sigma$ (mW)	99% (mW)	T (ms)	$\mu$ (mW)	$\sigma$ (mW)	99% (mW)	T (ms)	$\mu$ (mW)	$\sigma$ (mW)	99% (mW)
c1355	39	6.69 (+0.2%)	1.63 (-3.0%)	10.15 (-3.1%)	18 (6.9X)	6.67 (-0.3%)	1.66 (-1.2%)	10.39 (-1.7%)	124	6.68	1.68	10.57
c1908	32	9.93 (-0.1%)	2.07 (-2.8%)	15.16 (-0.7%)	17 (6.9X)	9.95 (+0.1%)	2.05 (-3.8%)	15.09 (-1.1%)	118	9.94	2.13	15.28
c3540	46	20.27 (-1.2%)	3.99 (-2.2%)	28.39 (-3.9%)	20 (6.4X)	20.30 (-1.1%)	4.04 (-1.0%)	28.37 (-3.6%)	128	20.52	4.08	29.43
c6288	43	30.37 (-0.4%)	6.70 (-3.6%)	43.35 (-2.0%)	21 (6.0X)	30.40 (-0.3%)	6.81 (-1.9%)	43.91 (-0.7%)	126	30.48	6.95	44.23
c7552	45	45.71 (-0.2%)	10.41 (-4.5%)	67.78 (-2.6%)	23 (5.9X)	45.72 (-0.2%)	10.72 (-1.8%)	68.52 (-1.4%)	135	45.82	10.92	69.62
ave	-	0.4%	3.3%	2.2%	20 (6.3X)	0.2%	2.1%	1.4%	127	-	-	-

number of variation terms is  $K = n^2 + 3n + 1 + 4ng_s$ . In the same way as that in the previous section, the computational complexity of full-chip-leakage-power calculation considering spatial variation is  $\mathcal{O}\{(n^2 + ng_s)N_t + (n^2 + ng_s)^2\}$ , and the computational complexity of incremental leakage-power calculation is  $\mathcal{O}\{(n^2 + ng_s)^2\}$ . On the other hand, in this case, the computational complexity of Wilkinson's approach is  $\mathcal{O}\{ng_s N_t^2\}$ , and that of incremental leakage-power calculation is  $\mathcal{O}\{ng_s N_t\}$ . We can see that, when  $N_t \gg g_s \gg n$ , our method is  $N_t$  times faster than Wilkinson's approach. That is, the efficiency improvement of our method is even higher when we consider spatial variation.

Handling within-die variation needs to calculate the expansion of polynomials, which is time consuming. However, such an operation needs to be run only once for all types of cells. Therefore, it will not increase the computational complexity.

## V. EXPERIMENTAL RESULTS

In the first set of experiments, we calculate leakage power for seven Microelectronics Center of North Carolina (MCNC) benchmarks [10]. For each benchmark, we implement it using a field-programmable gate-array (FPGA) circuit with lookup-table size = 4. For variation

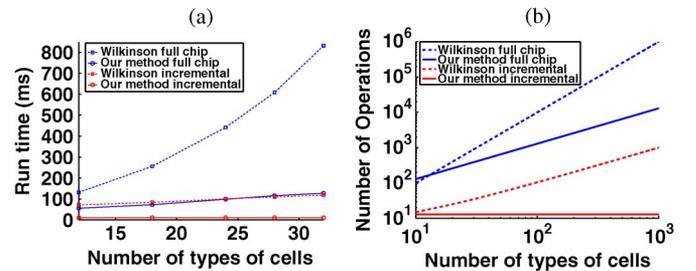


Fig. 1. (a) Run-time comparison for c1908 with varying numbers of cell types. (b) Estimated number of operations with varying numbers of cell types.

analysis, we assume two variation sources, namely, channel gate length and dopant density. For each variation source, we consider both inter- and within-die variations. They follow a Gaussian distribution, and the  $3\sigma$  values of inter- and within-die variations are 8% and 6% of the nominal value, respectively. In our experiment, we assume an International Technology Roadmap for Semiconductors 32-nm high-performance technology and use a Model for Assessment of cmoS Technologies And Roadmaps-4 tool [11] to calculate leakage power. We also define two comparison cases: 1) Wilkinson's approach and

TABLE VI  
MEAN, STANDARD-DEVIATION, AND 99%-PERCENTILE-POINT COMPARISON FOR FULL-CHIP CALCULATION OF LEAKAGE POWER FOR ISCAS85 STANDARD CELL BENCHMARKS ASSUMING THE EXISTENCE OF SPATIAL CORRELATION

Bench mark	$N_t$	Our Method				Wilkinson				MC		
		$\mu$ (mW)	$\sigma$ (mW)	99% (mW)	T (ms)	$\mu$ (mW)	$\sigma$ (mW)	99% (mW)	T (ms)	$\mu$ (mW)	$\sigma$ (mW)	99% (mW)
c1355	39	6.89 (+0.0%)	1.73 (-3.9%)	10.12 (-4.0%)	275 (23X)	6.90 (+0.1%)	1.76 (2.2%)	10.36 (-2.1%)	5215	6.89	1.80	10.54
c1908	32	10.16 (-0.4%)	2.15 (-1.8%)	15.75 (-0.8%)	295 (21X)	10.18 (-0.2%)	2.20 (-1.4%)	15.81 (-0.4%)	4912	10.20	2.23	15.87
c3540	46	21.32 (-0.9%)	4.08 (-2.8%)	29.89 (-1.6%)	328 (23X)	21.42 (-0.4%)	4.14 (-1.2%)	30.01 (-1.2%)	6538	21.50	4.19	30.36
c6288	43	32.11 (-0.3%)	6.86 (-2.3%)	45.35 (-1.7%)	371 (24X)	32.14 (-0.2%)	6.93 (-1.3%)	45.75 (-0.8%)	8675	32.20	7.02	46.12
c7552	45	46.84 (-0.2%)	10.69 (-3.9%)	69.42 (-1.8%)	397 (23X)	46.83 (-0.2%)	10.93 (-1.7%)	69.83 (-1.2%)	9702	46.93	11.12	70.68
ave	-	0.3%	3.1%	1.8%	331 (22X)	0.2%	1.6%	1.0%	7178	-	-	-

2) 10 000-sample Monte Carlo simulation. In the experiment, there are 17 types of circuit elements in the FPGA circuit. We implement all methods using MATLAB.

Table II compares the mean, standard deviation, 99% percentile point, and run time. In the table, the error percentage of mean, variance, and 99% percentile point is calculated as the error compared to that of Monte Carlo simulation, and the run-time speedup is calculated as the speedup of our method compared to that of Wilkinson's approach; average error is the average of the absolute value of error percentage. From the table, we can see that our method is five times faster than Wilkinson's approach while having no accuracy loss in mean estimation and about 1% accuracy loss in standard-deviation and 99%-percentile-point estimations.

Table III compares the incremental leakage-power calculation after changing one circuit element. From the table, we can also see that our method is five times faster than Wilkinson's approach with only a little accuracy loss.

We observe similar results in our application-specific integrated-circuit (ASIC) experiments. For the ASIC benchmarks, we use Predictive Technology Model (PTM) 45-nm technology. We consider one variation source, namely,  $L_{\text{eff}}$ . For  $L_{\text{eff}}$ , we assume that it follows a Gaussian distribution, and the  $3\sigma$  values of inter- and within-die variations are 8% and 6% of the nominal value, respectively. Table IV illustrates the comparison of mean, standard deviation, and 99% percentile point for full-chip-leakage-power calculation, and Table V shows those for incremental leakage-power calculation. From the tables, we find that our method is much faster than Wilkinson's approach with little accuracy loss.

Fig. 1(a) shows the run times for full-chip and incremental leakage-power calculations for c1908 under different numbers of cell types. From the figure, we see that our method is much more efficient than Wilkinson's approach when the number of cell types increases.

To further show the efficiency of our approach, we also estimate the number of operations for a larger standard cell library. Fig. 1(b) compares the estimated number of operations to compute full-chip leakage power and recalculate leakage power when one circuit element is changed under different standard-cell-library sizes. From the figure, we see that, when the size of the standard cell library is up to 1000, our method can achieve 100 times speedup when calculating full-chip leakage power and ten times speedup when recalculating leakage power compared to Wilkinson's approach.

Other than the aforementioned experiment, we have also done some experiments assuming the existence of spatial correlation. In the experiments, we assume that the  $3\sigma$  values of interdie, within-die spatial, and within-die random variations are 8%, 4.2%, and 4.2% of the nominal value, respectively. For spatial variation, we apply the grid-based spatial-variation model in [12], and we divide each chip into four grids. Table VI shows the results of the full-chip leakage power with the existence of spatial correlation. From the table, we find that our approach is 22 times faster than Wilkinson's approach with less than 2% accuracy loss. This validates the prior finding that

the efficiency improvement of our method is higher when we consider spatial variation, as discussed in Section IV.

## VI. CONCLUSION

The polynomial approximation of leakage power provides a deceptively simple, quick, and fairly accurate solution to calculate chip-leakage-power variation. Since only simple polynomial addition has been used, the method is very scalable, as well as incremental. It has been shown that, in order to recalculate chip-leakage-power variation after changing some circuit elements, the computational complexity of our approach does not depend on the number of circuit-element types (standard-cell-library size), while the complexity of Wilkinson's approach, which is widely used in many existing statistical leakage analysis works, is linear to the circuit-element types. Experimental results have shown that our method is five times more efficient than Wilkinson's approach with no accuracy loss in mean estimation and about 1% accuracy loss in standard-deviation and 99%-percentile-point estimations.

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