

Device- and Circuit-Level Variability Caused by Line Edge Roughness for Sub-32-nm FinFET Technologies

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Abstract—The variability impact of line edge roughness (LER) on sub-32-nm fin-shaped FET (FinFET) technologies is investigated from both device- and circuit-level perspectives using computer-aided design simulations. Resist-defined FinFETs exhibit sizeable device performance variation (up to 10% fluctuation in threshold voltage and 200% in leakage current) when subjected to fin roughness up to 1 nm root-mean-square amplitude. Spacer-defined FinFETs show negligible device performance variation and exhibit quadratic dependence with LER amplitude. For both patterning technologies, the resulting impact on large-scale digital-circuit performance variation is found to be minimal in terms of the overall delay mean and variation. This is attributed to self-averaging of uncorrelated LER effects between individual devices within the circuits, resulting in minimal delay impact for digital-circuit design. The impact of LER on leakage power variation is also found to be minimal for all technologies; however, the mean value increases by up to 40% for 15-nm resist FinFETs. On this basis, the impact of LER on sub-32-nm FinFET device-level variability is only significant for resist devices, whereas the resulting digital-circuit impact is important only in terms of mean leakage power increase.

Index Terms—Device scaling, fin-shaped FET (FinFET), line edge roughness (LER), spacer-defined patterning, variability.

I. INTRODUCTION

VARIABILITY is becoming a significant obstacle to CMOS scaling in the deep submicron-to-nanometer regime. As feature sizes shrink, random fluctuations in device geometry and composition utilize more and more of the allowed variability budget that results from processing. These device-to-device fluctuations may arise from a number of variability sources including line edge roughness (LER) and/or line width roughness (LWR), random dopant fluctuations (RDFs), oxide thickness fluctuations, work-function variation, etc. As a result, the performance of individual devices becomes random and unpredictable, leading to a statistical distribution in parameters such as threshold voltage V_T , ON-state drive current I_{on} , OFF-state leakage current I_{off} , subthreshold swing (SS), and drain-induced barrier lowering (DIBL). This can be particularly

troublesome in circuit applications where precise device matching is critical.

Fin-shaped FETs (FinFETs) [1] are regarded as one of the most attractive candidates for postplanar CMOS scaling beyond the 32-nm node due to their excellent short-channel-effect control [2]. Moreover, the use of undoped fin bodies and gate work-function engineering makes FinFETs highly robust against RDF variability. Unfortunately, the 3-D structure of FinFETs makes them highly susceptible to performance degradation and variability due to LER. To date, however, only a limited number of studies [3]–[12] exist on LER-induced FinFET variability, most of which only focus on a single technology generation and/or LER value or a limited number of device performance figures (e.g., threshold voltage and drive current). A selected number of FinFET circuit-level variability studies have been conducted; however, most are relegated to a single memory/logic cell level [4], [5], [9], [11], [13], small size circuits [14], [15], or analog matching [8], [9].

In this transaction, we explore the impact of LER and technology scaling on double-gate FinFET variability from both an individual device perspective and a large-scale digital-circuit, i.e., microprocessor, perspective. Our simulation results show that fin-sidewall LER up to 1 nm has a sizeable impact on the device performance for resist-defined FinFETs, whereas spacer-defined FinFETs are negligibly impacted. However, due to the averaging effect of LER between different devices, we find that, for both resist- and spacer-FinFET technologies, the resulting impact on digital-circuit performance variability is largely negligible. The main driver for LER in large-scale digital-circuit design will likely be the significant increase in mean leakage power.

II. LER AND FinFET DEVICE MODELING

A. LER Modeling

Gaussian LER patterns are generated using the 1-D Fourier synthesis approach described in [16] and are used to augment the fin-edge positions in the FinFET structures. The Gaussian model is chosen for reasons that will be explained next. Surface smoothing treatments such as thermal annealing [17], [18], sacrificial oxidation [19], and resist trimming [20] are capable of eliminating the majority of high-frequency roughness. Moreover, it has been shown [4] that low-frequency roughness is the more significant source of intradie variability characteristic of

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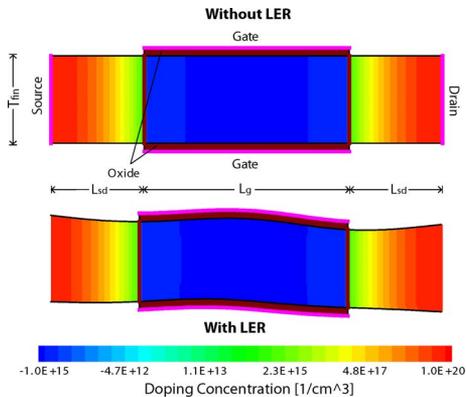


Fig. 1. Schematic of the 2-D structure used to model the n-type double-gate FinFET devices (32-nm case shown) with and without fin LER. The structure shown represents a planar cut across the height of the fin and parallel to the plane of the wafer. Current flows strictly within the plane, i.e., from right to left.

LER. With this in mind, we sought a simple analytical form having a power spectrum consisting of mostly low-frequency roughness and negligible contribution from higher frequencies, leading us to choose the Gaussian model.

In our simulations, we varied the root-mean-square roughness amplitude σ_{LER} from 0 to 1 nm to represent typical LER values, which may be required by the industry heading beyond 32-nm technology, based on the 2009 International Technology Roadmap for Semiconductors (ITRS) [21] forecast and experimental data [16]. We fixed the correlation length $\lambda = 15$ nm since previous studies [4], [6] have shown that the effect of λ diminishes as $\lambda > 15 - 20$ nm, and some experimental data have shown that current values of λ are estimated between 20 and 30 nm [16] and generally reduce with technology, suggesting $\lambda = 15$ nm as a reasonable estimate for sub-32-nm lithography.

B. FinFET Design and Modeling

The FinFET devices used in this paper are designed to meet the 2009 ITRS targets for high-performance logic multigate devices at the 32-, 21-, and 15-nm nodes. As of this writing, FinFETs are not being implemented at 32-nm, but we still include the 32-nm node for a detailed comparison. The n-type double-gate FinFETs are modeled in Sentaurus technology computer-aided design (TCAD) using a 2-D framework, as depicted in Fig. 1. Because of the purely double-gate structure, there is perfect symmetry along the fin-height direction, i.e., no z -directed electric field; thus, computationally efficient 2-D simulations can be employed. The upper FinFET represents the nominal case where no LER is present, whereas the lower FinFET includes LER along the fin sidewalls only (i.e., fin LER) causing fluctuation of the fin thickness along the channel. The effect of gate LER is not explicitly considered in our paper since previous works indicate that it is less detrimental than fin LER for devices with small fin widths, but its impact may be assumed to add in an uncorrelated fashion [4]–[7]. A fin body doping of 10^{15} cm^{-3} is used to represent an undoped or intrinsic fin, since the presence of a single dopant already quantizes the minimum doping to roughly 10^{18} cm^{-3} . The

TABLE I
NOMINAL PARAMETERS FOR SIMULATED FinFETs

Quantity	Node			Description
	32nm	21nm	15nm	
L_g (nm)	22	17	13	Physical gate length
EOT (nm)	0.90	0.77	0.64	Equiv. oxide thickness
N_A (cm^{-3})	10^{15}	10^{15}	10^{15}	Body/fin doping
T_{fin} (nm)	9.6	8	6.4	Fin thickness
L_{sd} (nm)	10	8	6	S/D extension length
σ_{SD} (nm/dec)	1.3	0.8	0.5	S/D doping gradient
ψ_M (eV)	4.47	4.47	4.47	Metal gate work function
V_{DD} (V)	0.9	0.81	0.73	Power supply voltage
$V_{T,\text{lin}}$ (mV)	272	282	298	Lin. threshold voltage
$V_{T,\text{sat}}$ (mV)	201	203	208	Sat. threshold voltage
I_{on} ($\mu\text{A}/\mu\text{m}$)	1432	1527	1734	On-state drive current
I_{off} (nA/ μm)	6.7	9.7	13.3	Off-state leakage current
SS (mV/dec)	67.9	69.8	71.6	Subthreshold swing
DIBL (mV/V)	24.0	32.0	39.7	Drain-induced, bar. low.

$V_{T,\text{lin}}$ is extracted by the maximum g_m method with $V_{\text{DS}} = 50$ mV.

$V_{T,\text{sat}}$ is extracted by the current method at $W/L_g \times 10^{-7}$ A with $V_{\text{DS}} = V_{\text{DD}}$.

I_{on} is defined at $V_{\text{DS}} = V_{\text{GS}} = V_{\text{DD}}$.

I_{off} is defined at $V_{\text{DS}} = V_{\text{DD}}$ and $V_{\text{GS}} = 0$.

availability of a suitable high- κ metal gate stack is also assumed so that an equivalent oxide thickness can be substituted while neglecting oxide tunneling leakage and using work-function tuning to adjust the V_T values. A calibrated hydrodynamic transport model is used to model current flow in the short-channel FinFETs without having to resort to expensive Monte Carlo simulations [22], [23]. Furthermore, quantum corrections are taken into account by the density-gradient approximation. The nominal device parameters used in the simulated FinFETs are listed in the upper portion of Table I and are chosen to match the ITRS values as closely as possible.

III. LER IMPACT ON DEVICE VARIABILITY

A. Baseline Performance Values

The baseline performance figures for the ideal FinFETs are included in the lower portion of Table I. These numbers serve as the reference for comparison when studying the effect of fin LER on simulated device ensembles. As a reminder, gate LER is not considered in this paper. The variability in device performance is quantified by the standard deviation of each parameter listed in the lower half of Table I, expressed as a percentage of its baseline value. Unless otherwise indicated, the ensemble size is 200 devices for each (σ_{LER} , λ , and technology node) triplet.

B. Resist-Defined FinFET Variability

The LER impact on resist FinFETs is shown in Fig. 2 as a function of σ_{LER} . The moderate-to-large variation of $V_{T,\text{lin}}$ and $V_{T,\text{sat}}$ with LER is evident, particularly in the latter case where $\sigma V_{T,\text{sat}}$ can exceed 10%. As expected, the 15-nm devices show the most variation, whereas the 32-nm devices show the least. The threshold voltage variation linearly depends on σ_{LER} since the total depletion charge in a fully depleted FinFET is directly impacted by fin-thickness fluctuations, i.e., the fin LER. This amount of LER-induced V_T variation may be troublesome in circuits requiring precise threshold voltage matching. Similar levels of the V_T variation due to fin LER have been also found in [4] and [7].

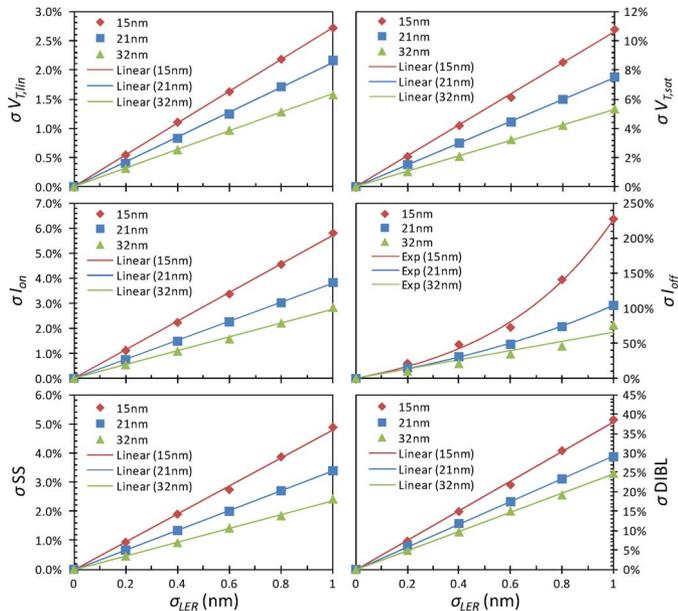


Fig. 2. Resist-FinFET device variability as a function of LER amplitude and technology node. (Markers) Actual simulated data. (Solid lines) Best fits.

The I_{on} variation exhibits a similar but weaker dependence considering that σI_{on} can be easily kept within 10% of the nominal value in each technology node up to $\sigma_{LER} = 1$ nm; similar findings have been also reached in [4] and [7]. Note that σI_{on} is also linear with σ_{LER} since the drive current is linearly proportional to $V_{DD} - V_T$ in velocity-saturated FETs. The variation of I_{off} is much more pronounced, however, where σI_{off} exponentially varies with σ_{LER} (since I_{off} is an exponential function of V_T) and reaches more than 200% of the nominal value for 15-nm devices. Such wild fluctuations in I_{off} may be detrimental to circuit performance if the power dissipation of individual devices and circuit blocks cannot be kept within acceptable margins. In light of these results, it appears that the drastic variation of I_{off} due to fin LER may be a critical obstacle toward the further scaling of FinFETs beyond 32-nm.

The effect of LER on the SS is somewhat low on the order of a few percent and is also linear since the fluctuation of T_{fin} due to $\sigma_{LER} \leq 1$ nm can be treated as a linear perturbation in C_D , i.e., $C_D = \epsilon_{Si}/(T_{fin} + \Delta T_{fin}) \approx \epsilon_{Si}/T_{fin}(1 - \Delta T_{fin}/T_{fin})$, where ΔT_{fin} is roughly given by σ_{LER} . The DIBL variation is more considerable, i.e., $\sigma DIBL$ easily exceeds 10% in each generation over the LER range, as opposed to the SS variation, which can be kept under 10% for the entire LER range.

C. Spacer-Defined FinFET Variability

For spacer FinFETs, the impact of LER is drastically reduced in terms of parameter fluctuations for all three technology generations, as revealed in Fig. 3. Note the zoomed vertical scales used in Fig. 3 for spacer FinFETs compared with those in Fig. 2 for resist FinFETs. From the data, the elimination of LWR by spacer lithography (due to sidewall correlation) offers substantial improvement in minimizing device variation. These results compare well with the findings in [4], which demon-

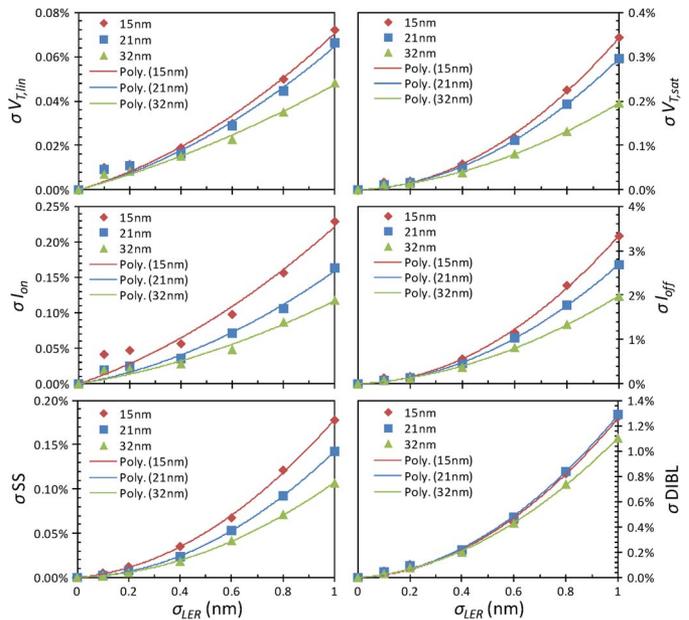


Fig. 3. Spacer-FinFET device variability as a function of LER amplitude and technology node. (Markers) Actual simulated data. (Solid lines) Best fits. Note: The scale here is highly zoomed, as compared with Fig. 2.

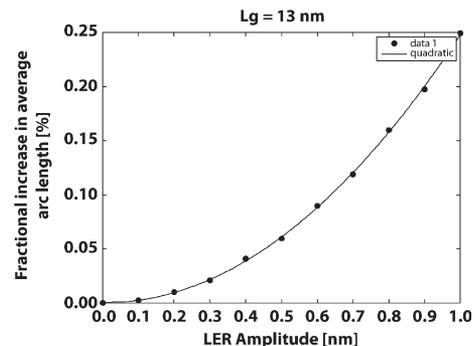


Fig. 4. Quadratic rise in the average arc length for spacer FinFETs due to LER as a function of the root-mean-square roughness amplitude. The nominal arc length corresponds to a 13 nm channel length for the data shown.

strate a significant reduction in saturation threshold voltage mismatch and current factor mismatch to less than 1% of the nominal values over a similar LER range. We also observe that, in most cases, the variability curves show less dependence on the actual technology node for spacer-defined FinFETs. In other words, there is little difference between the 32-, 21-, and 15-nm cases here. From this, we see that the presence (absence) of LWR is responsible for the observed variability trends in the resist (spacer) FinFETs, rather than the actual LER itself.

Interestingly, every parameter investigated appears to vary quadratically, rather than linearly, with σ_{LER} . To explain why, we first observe that, because of the correlated fin edges in a spacer FinFET, the body thickness does not change along the length of the fin, i.e., $\sigma_{LWR} = 0$. However, the presence of LER causes the body/channel region to bend and curve in shape which results in a curved potential profile compared with an ideal device, and hence, the path for the current should roughly follow the curvature of the fin geometry. Mathematically, the total arc length from the source to the drain can

TABLE II
NOMINAL DELAY AND CELL NUMBERS OF PROCESSOR BENCHMARKS

Benchmark	32nm		21nm		15nm	
	Delay [ps]	Cell count	Delay [ps]	Cell count	Delay [ps]	Cell count
M0 (fast)	512	8798	362	8331	222	7262
M0 (medium)	965	7224	775	7118	408	6809
M0 (slow)	1388	7050	935	7098	561	7034
MIPS (fast)	379	9975	280	7528	156	7779
MIPS (medium)	985	7369	563	6674	320	6288
MIPS (slow)	1482	6854	895	5893	617	5897

device performance figures. To resolve this artifact, we also extract second-order terms for these parameters and apply a compensating mean shift to those compact model parameters.

In this paper, we extract two sets of compact model samples to match the delay-related device performance figures (e.g., I_{on} , $V_{T,lin}$, $V_{T,sat}$, and DIBL) and leakage-related device performance figures (e.g., I_{off} , $V_{T,lin}$, $V_{T,sat}$, and SS).

D. Circuit-Level Variation Model and Circuit Simulation

To evaluate the impact of LER on large-scale digital circuits, we pick two full processor benchmarks: MIPS [31] and ARM Cortex-M0 [32]. In order to explore benchmark application varieties in speed and power, we synthesize, place, and route them at three different clock periods (fast, medium, and slow) using our baseline FinFET cell library (see Table II).

Because LER is stochastic, the impact between individual fins in all cells is assumed to be completely uncorrelated. We perform the Monte Carlo sampling in two steps. First, each device in the cell netlist is randomly substituted by one of the generated device samples from the previous PCA. The new cell library samples that contain these cells are characterized using library incremental characterization tools. Second, each cell in the benchmark netlists is randomly replaced by the cell from the cell library samples.

In this paper, we generate 60 device model samples, 100 netlist samples for each cell type, and 50 circuit netlist samples. The netlist samples are fed into conventional circuit analysis tools with the library samples for circuit delay and leakage analysis.

E. Circuit Simulation Results

Some of the simulation results¹ are highlighted in Table III. Because most of the delay variations are quite small, the standard deviation (sigma) values contain large amounts of quantization noise, as the raw delay values are rounded to 1 ps, which is the accuracy limit for the commercial timer [26]. In this section, we only report the most important leakage results, as well as those with relatively large delay variations.

1) *Resist-Defined Versus Spacer-Defined FinFETs*: Since LER is uncorrelated between devices, its impact tends to average out across different instances. Although LER has a significant impact on a device level for resist FinFETs, circuit simulations show that the same amount of LER has a much smaller impact on the corresponding circuit-level delay and

TABLE III
DELAY AND LEAKAGE MEAN AND SIGMA OVER ALL BENCHMARKS WITH 1-nm LER FOR RESIST (R)- AND SPACER (S)-FinFET TECHNOLOGIES

Node	Delay			Leakage		
	Baseline w/o LER	Mean w/ LER	Sigma w/ LER	Baseline w/o LER	Mean w/ LER	Sigma w/ LER
32-S		100%	0.00%		100%	0.0%
32-R	952 ps	101%	0.15%	14.65 μ W	114%	0.1%
21-S		100%	0.00%		100%	0.0%
21-R	635 ps	106%	0.30%	11.47 μ W	125%	0.1%
15-S		100%	0.01%		100%	0.0%
15-R	381 ps	102%	0.04%	6.59 μ W	149%	0.2%

Mean and sigma values have been normalized to their baseline (no LER) values and are averaged over all six benchmarks in Table II.

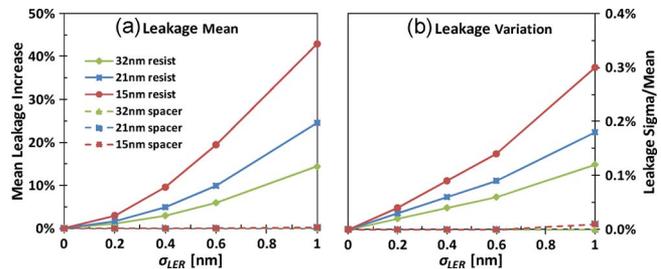


Fig. 6. (a) Increase in the mean leakage power and (b) variation of the leakage power as a function of the LER amplitude and the technology node for (solid) resist- and (dashed) spacer-defined FinFET circuit benchmarks.

TABLE IV
CRITICAL PATH LENGTH AND AVERAGE CELL SIZES FOR DIFFERENT 15-nm FinFET BENCHMARKS AT 1-nm LER SIGMA

Benchmark	Cells in the critical path (N)	Average sizes (X)	$\sqrt{\frac{N}{X}}$	Delay sigma [ps]
M0 (fast)	41	3.49	3.43	0.8
M0 (medium)	51	1.43	5.97	2.8
M0 (slow)	59	1.15	7.16	2.7
MIPS (fast)	32	5.75	2.36	0.6
MIPS (medium)	44	2.00	4.69	1.3
MIPS (slow)	53	1.15	6.79	1.9

power variability. Both delay and leakage have standard deviations less than 1% of their mean values for resist FinFETs (see Table III). For spacer FinFETs, the LER impact is virtually negligible.

2) *Technology Scaling*: The magnitude of circuit-level variability increases with more aggressive technology scaling. As shown in Table III, the circuit delay variation (in terms of sigma/mean) increases from 0.2% to 0.7% as the technology scales from 32- to 15-nm. As shown in Fig. 6(a), the normalized mean leakage shift increases from 14% to 43% for resist FinFETs as the technology scales from 32- to 15-nm, while the leakage variation increases from 0.12% to 0.3% for resist FinFETs as the technology scales from 32- to 15-nm. In summary, both the delay and leakage variations are almost negligible. However, the increase in mean leakage of up to 43% for resist FinFETs at 1 nm LER may be a concern for low-power applications.

3) *Benchmark Variability*: Different circuit benchmarks show similar impacts from LER but with slightly different vulnerability (see Table IV). Because the effect of LER averages across all devices along the critical path, a simple vulnerability metric of the critical path delay to LER is $(N/X)^{1/2}$, where N is the critical path depth and X is the average cell size in the critical path. Because LER has little impact on the circuit delay,

¹The entire set of data is available online at :http://nanocad.ee.ucla.edu/pub/Main/Mfd/LER_circuit_data.xlsx

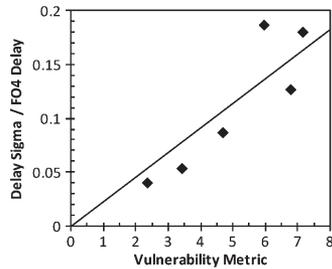


Fig. 7. Correlation of the vulnerability metric with delay sigma (normalized to the fan-out of four inverter delay of 15 ps) for the six 15-nm FinFET benchmarks investigated in Table IV at 1 nm LER amplitude.

the total number of possible critical paths in this case is small. For larger variations, a similar method in [29] can be applied to account for different possible critical paths. From Fig. 7, the processor delay results correlate with this metric.

Unlike the common intuition that fast circuits are more susceptible to local variations, in some cases, they are less susceptible to purely stochastic variability sources such as LER. For example, circuit designers can make circuits operate faster by using larger size cells, which make them more resilient to LER. Shortening the critical path length can also reduce their absolute variation (sigma) values due to LER, but it may also increase their relative variation (sigma/mean) values at the same time.

F. Implications for LER Targets

The circuit-level impact of LER is highly application specific. For static random access memory or analog circuits, LER can cause severe problems for circuit matching [4], [9], [11], whereas for large-scale digital circuits, LER-induced variability is found to be virtually negligible even for 15-nm resist FinFETs subjected to 1 nm LER. The primary concern for LER in digital logic is likely to be the increase in mean leakage, which is more than 40% for 15-nm resist FinFETs for LER up to 1 nm. Extrapolation of the data in Figs. 2, 3, and 6 may be used to obtain a specific estimate on the maximum tolerable LER amplitude (i.e., process technology) that meets a designer's variability budget.

V. CONCLUSION

Using TCAD simulations, we have found that the impact of LER up to 1 nm amplitude is nonnegligible for resist-defined FinFETs and negligible for spacer-defined FinFETs starting from the 32-nm node. Fluctuations in threshold voltage, leakage current, and DIBL were significant across the range of design targets studied. Furthermore, the evolution of device performance variability versus LER amplitude for spacer-defined FinFETs has been revealed to be quadratic in nature, which contrasts to the linear nature seen in resist-defined FinFETs. We have also evaluated the LER impact on different circuit benchmarks. Our results have shown that the variability introduced by LER on circuit performance is similar to that on device performance but with much smaller magnitude. The simulation results show that different digital-circuit benchmarks have different vulnerability to purely random variations

such as LER. Digital-circuit delay and leakage were minimally impacted by LER except for an increase in mean leakage power of up to 40% for 15-nm FinFETs. Based on these findings, sub-32-nm FinFETs may be useful in large-scale microprocessor applications despite their susceptibility to LER-induced device variability.

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