Technology Path-finding for Directed Self-Assembly for Via Layers

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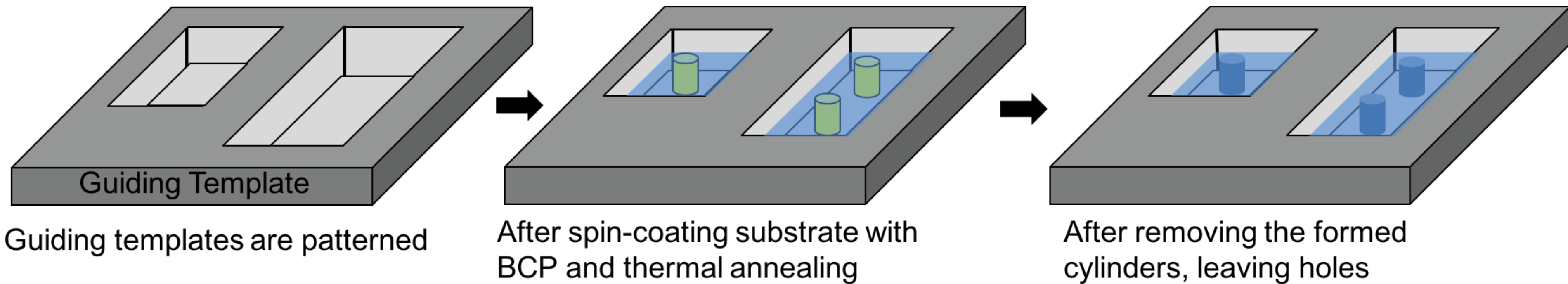
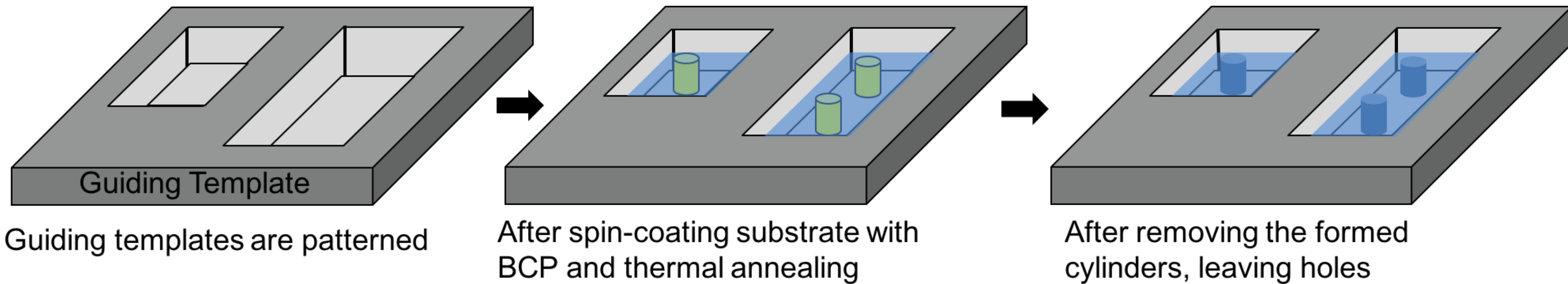
A Design-friendly DSA-based Technology



A DSA-based technology:

Complementary Lithography + Block Copolymer

A Design-friendly DSA-based Technology



For a Design-friendly technology:

Which type(s) of complementary Lithography?

How many masks/exposures?

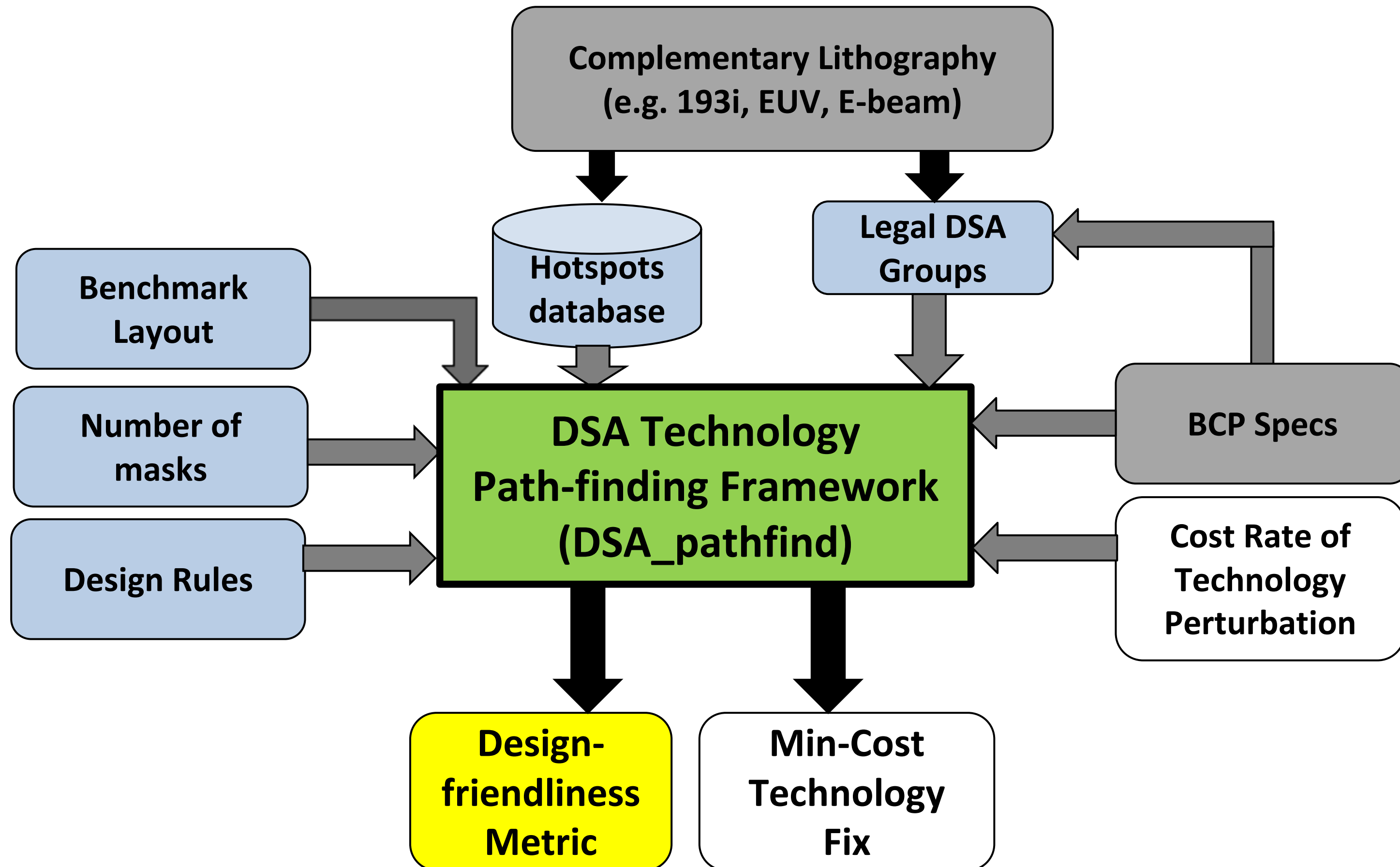
Which guiding templates are important?

Which Block Copolymer?

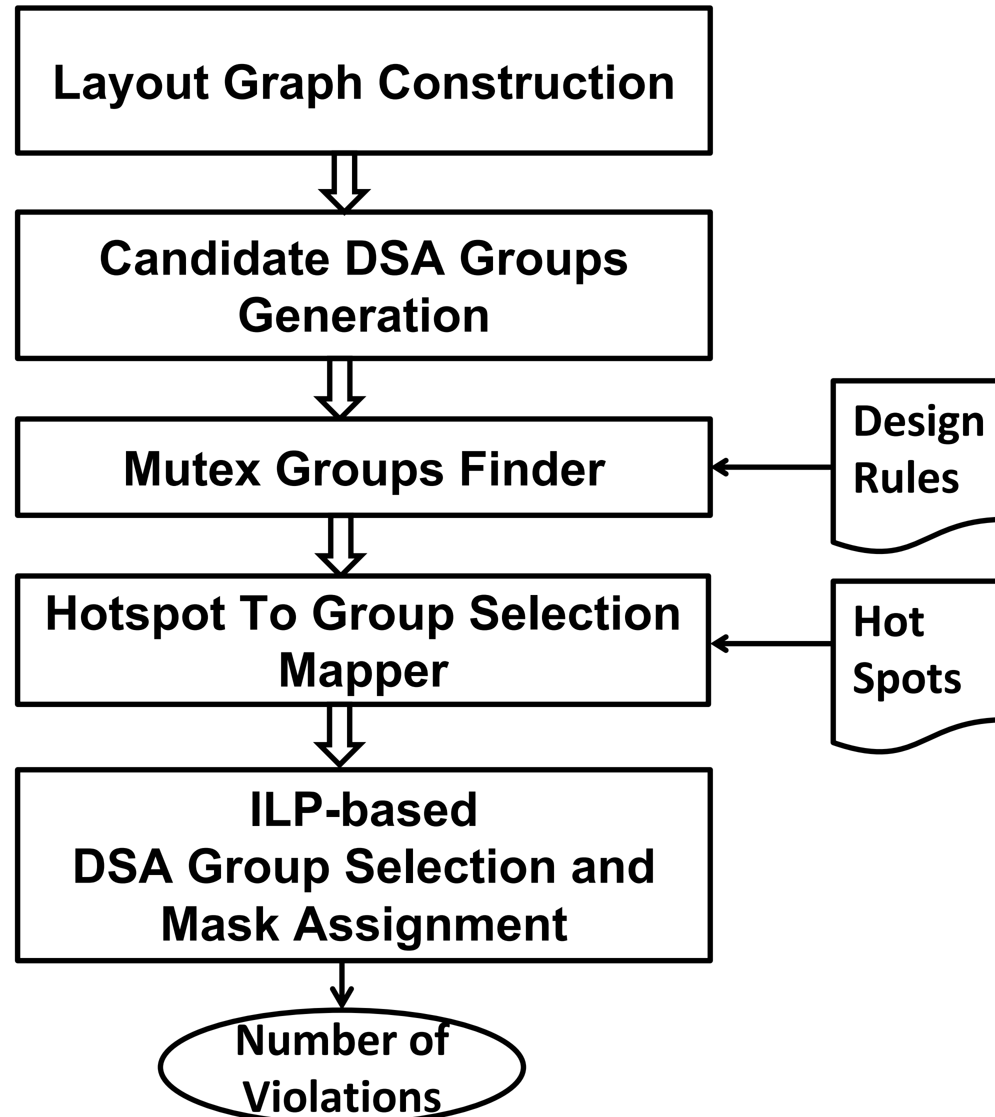
Previous Work

1. **Heuristics for DSA Grouping + MP decomposition**
   – E.g. Badr et al; DAC'16
2. **Improving robustness of self-assembly**
   – E.g. selection of the BCP and the guiding template dimensions as in *Ma et al, JM3' 16*
3. **Technology Exploration for DSA+MP**
   – *Karageorgos et al., JM3'16*:
   - Optimal method (based on enumerating solutions) only works for small cluster ~15 vias
   - Heuristics for larger clusters

Overview of the Framework

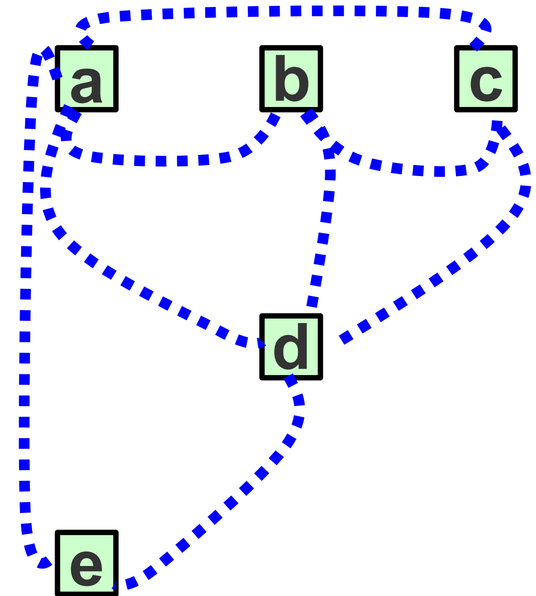


Flow of the Framework

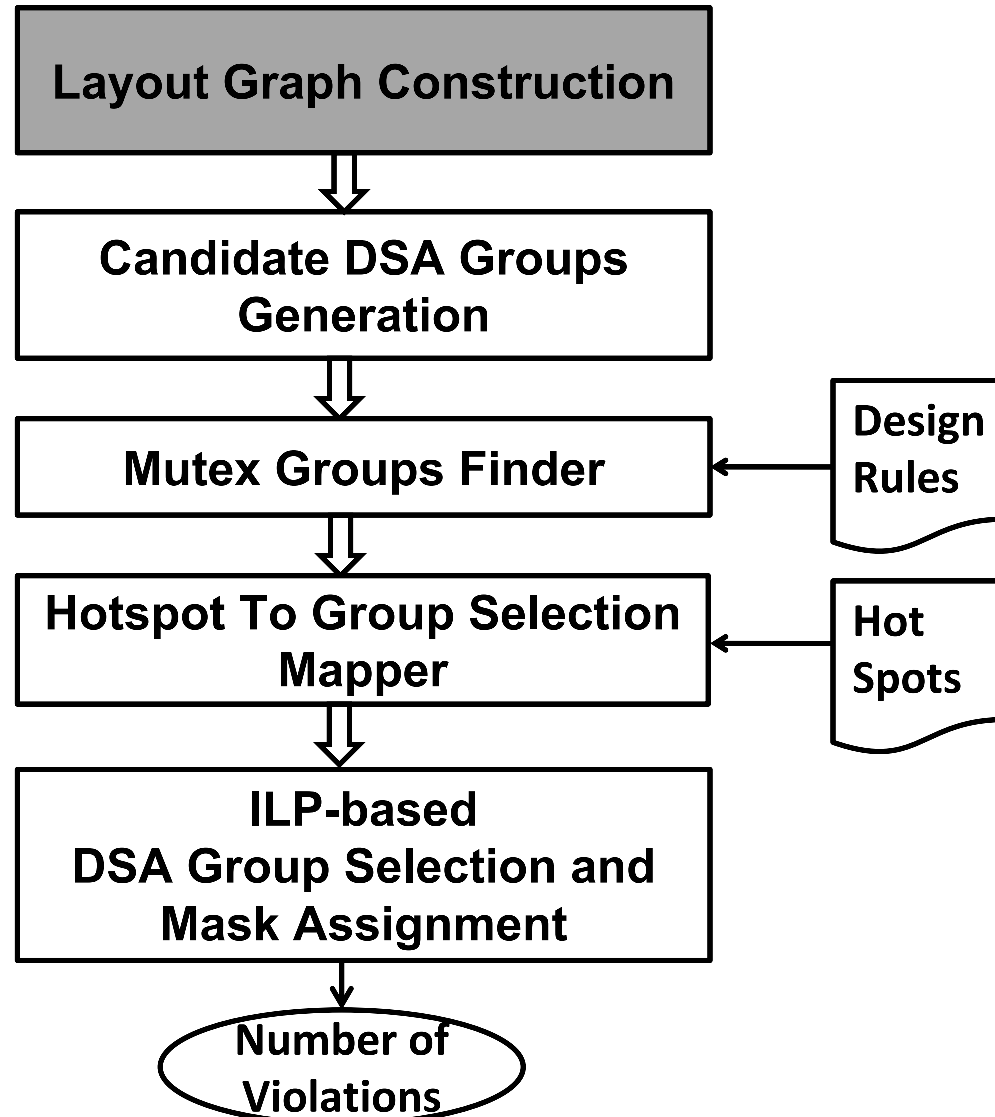


Layout Graph Construction

- **Graph node:** for every via
- **Spacing Edge**: between every pair of contacts whose center-to-center distance is less than *min_pitch_same_mask*
- *O(n)*

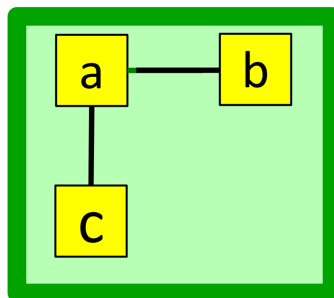


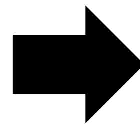
Flow of the Framework

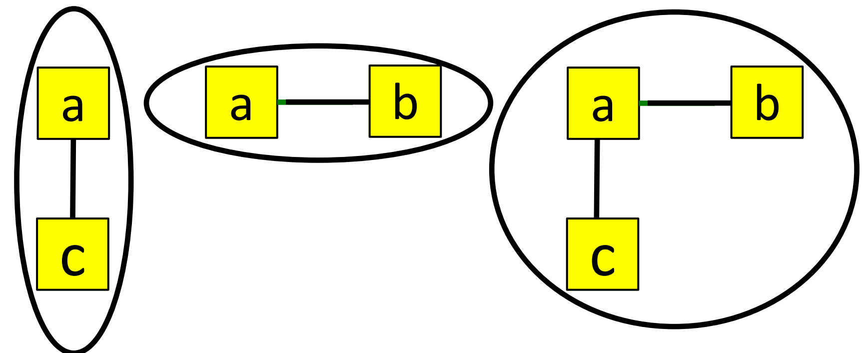


Candidate DSA Groups Generation

1. Finding Grouping Options
   - ***Depth-first Graph traversal*** *→enumerate connected subgraphs smaller than maxG*
     - *maxG is* maximum number of vias per group, due to DSA yield issues.
     - O(n), assuming small *maxG*



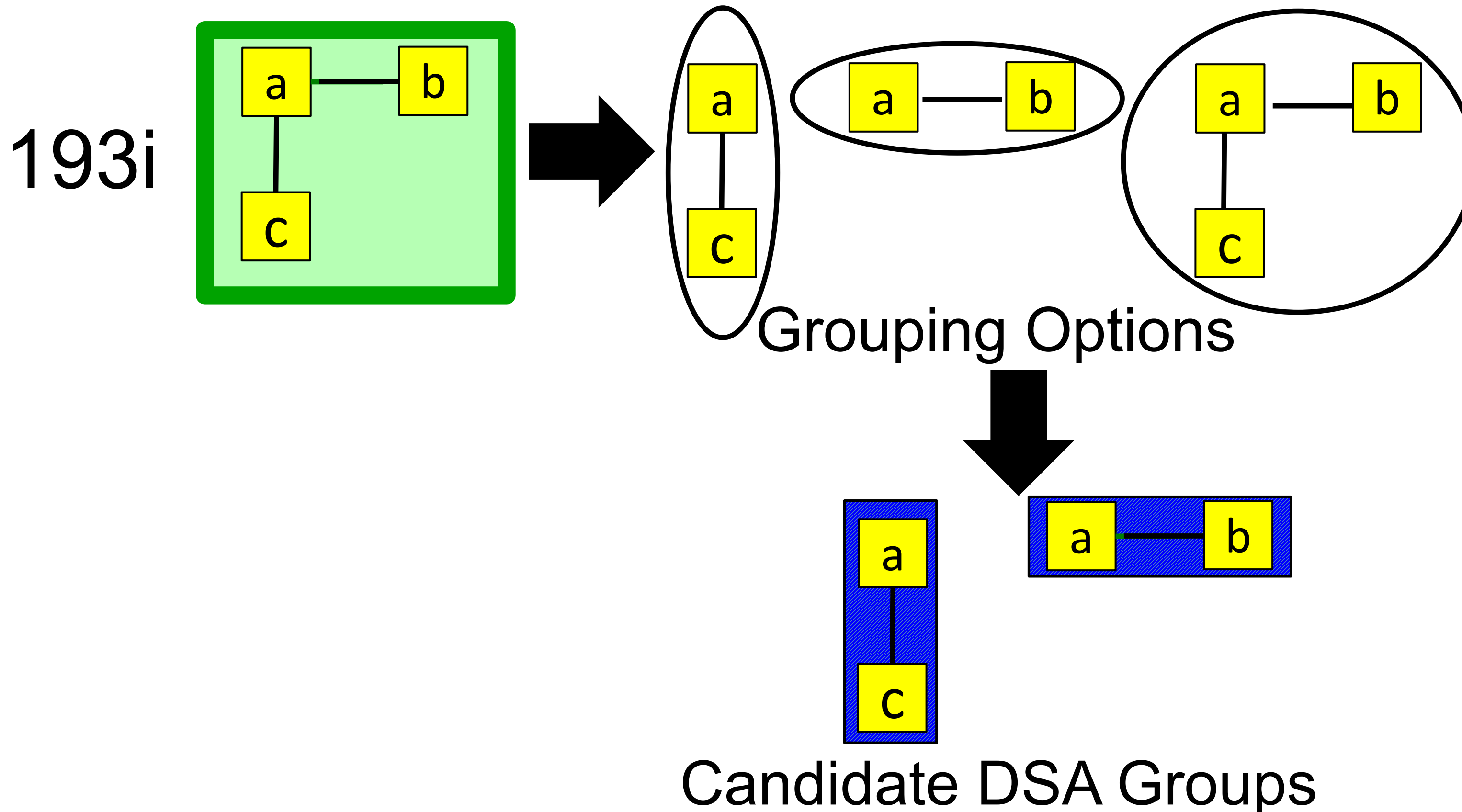




Grouping Options

Candidate DSA Groups Generation

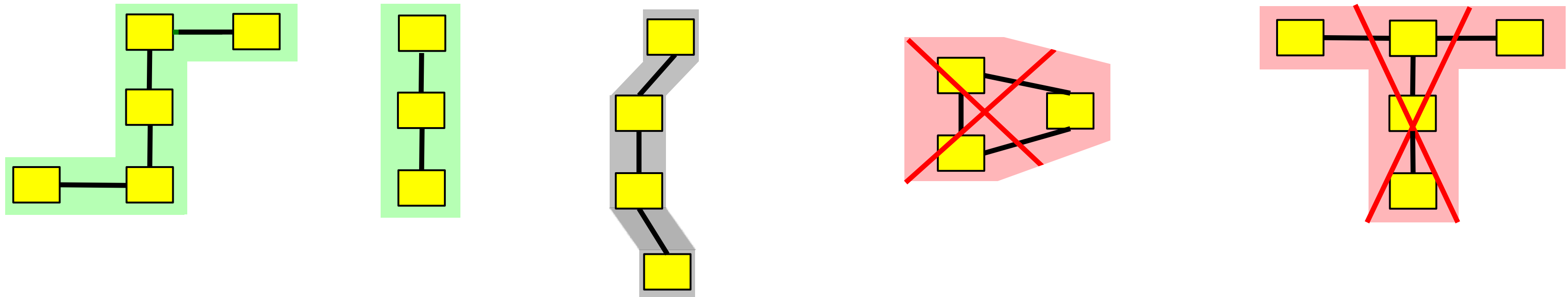
2. Finding Candidate Groups
   – Uses a **grouping checker** that is specific to the complementary lithography under evaluation



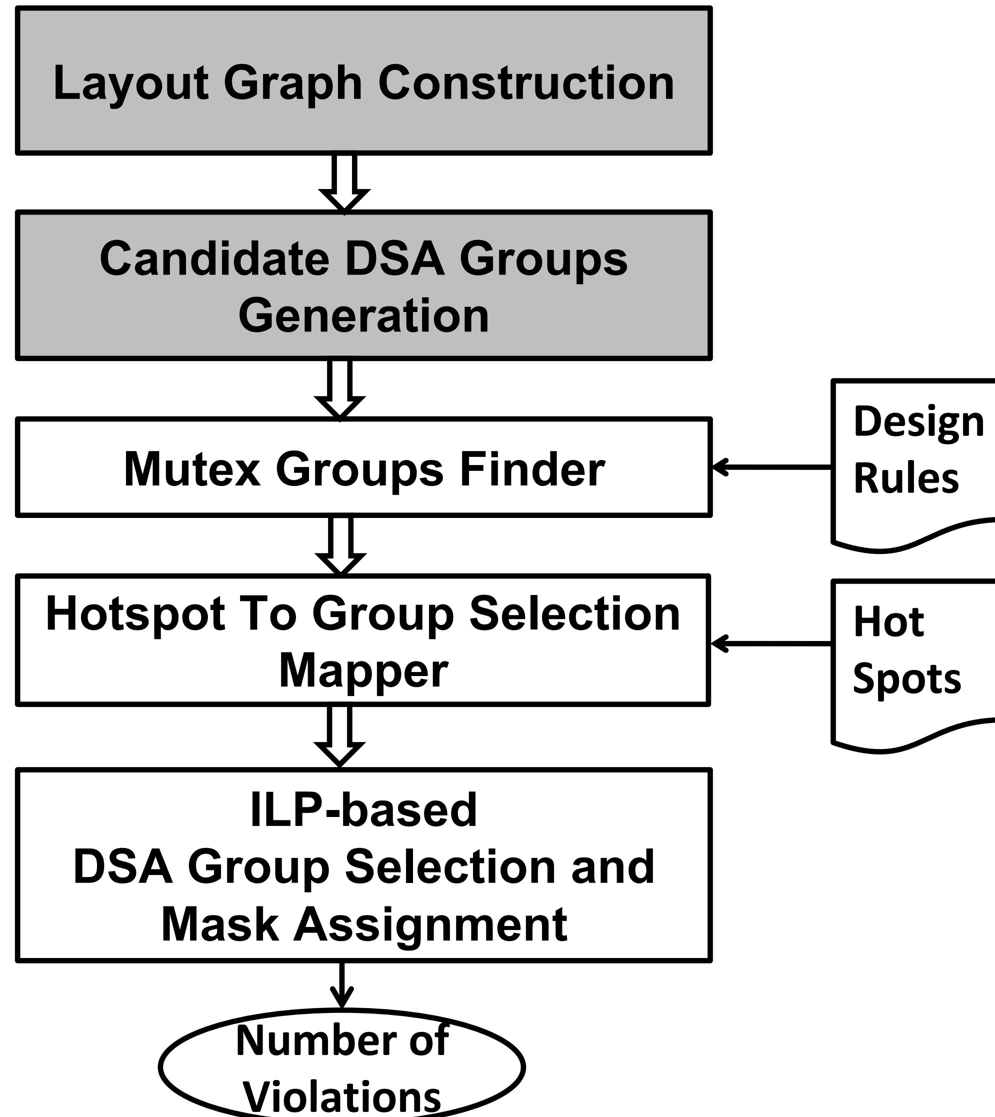
Candidate DSA Groups Generation

2. Finding Candidate Groups
   – Uses a **grouping checker** that is specific to the complementary lithography under evaluation

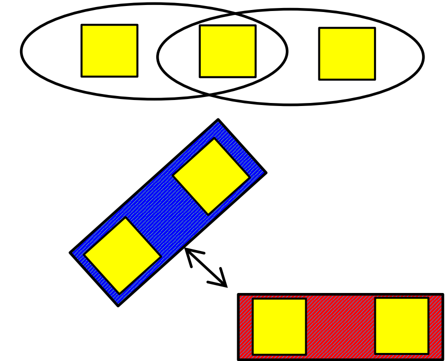
- Grouping Checkers
  – Given a set of vias, decide if they form a legal DSA group
  – Example: EUV Grouping Checker

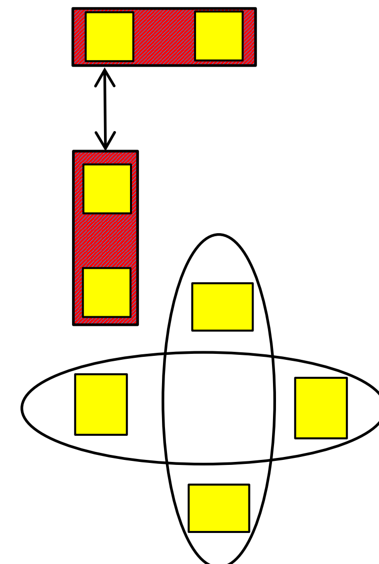


Flow of the Framework



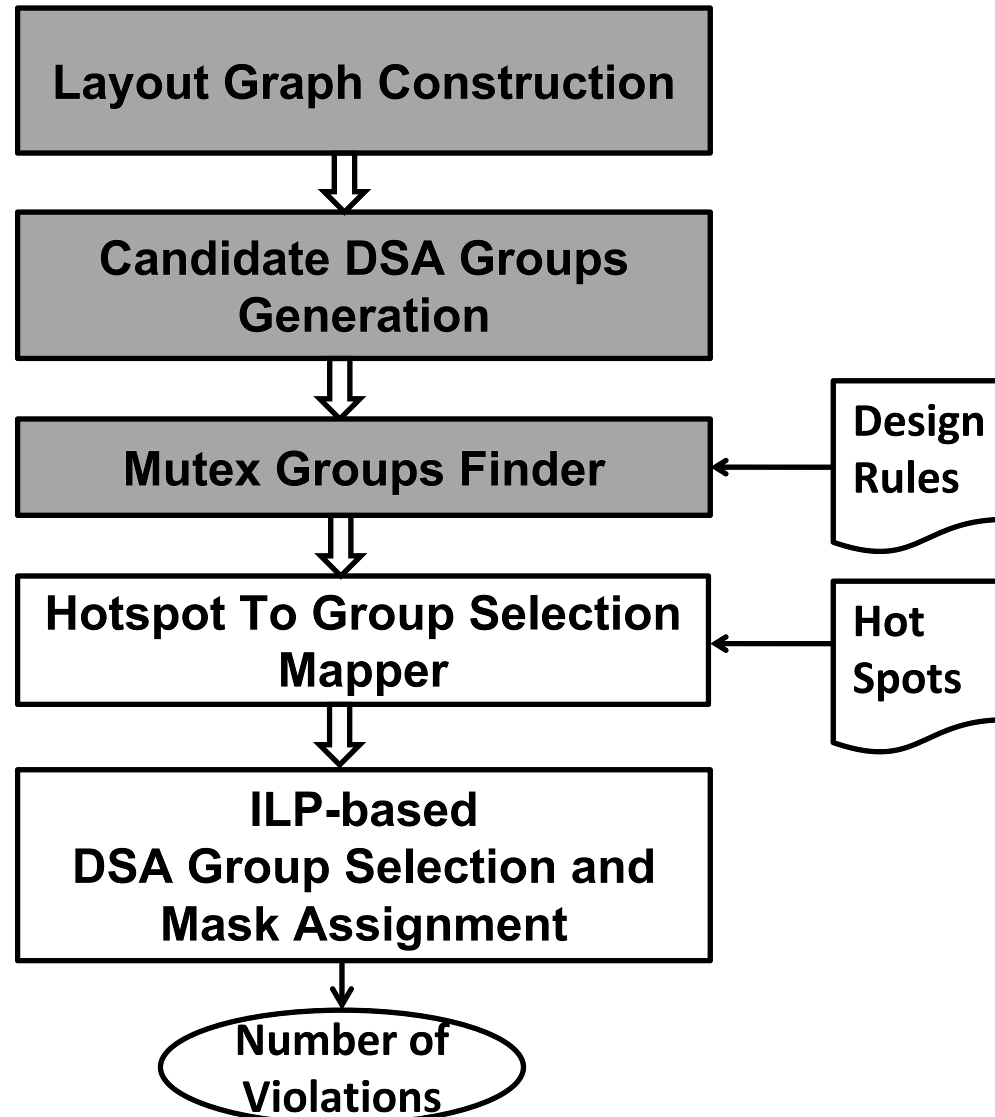
Mutually Exclusive Groups Finder





- Why **Mutex groups**?
  - Have one or more common via
  - Distance < ***min_pitch_diff_mask***
    ➔ **only one** of them can be selected
  - Distance < ***min_pitch_same_mask***
    ➔ the **two groups** (if selected) must be assigned to **different masks**
  - Templates **overlap geometrically**
    - May or may not be forbidden based on process
- $O(n^{1.5})$

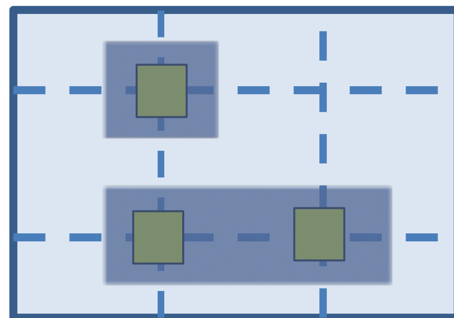
Flow of the Framework



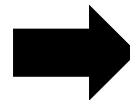
Hotspot to Group Selection Mapper

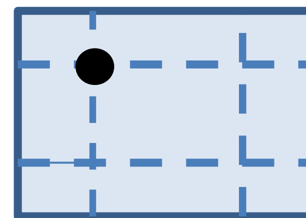
- A **hotspot** can be:
  - Lithography hotspot
  - Complex 2D design rules (pattern-based design rules)
  - Patterns that are forbidden in a restrictive technology (example: SADP)

- Each hotspot can have a different dimension (up to 5x5)

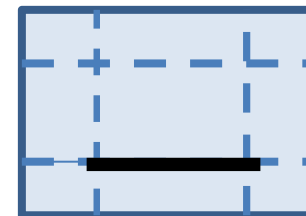


Similar to representation used in Badr et al. JM3'14





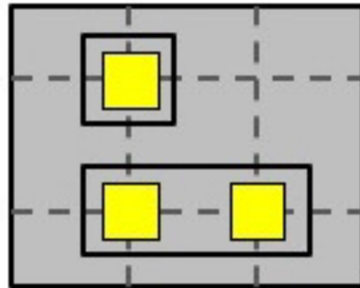
Singletons Representation
0010→ 0x02



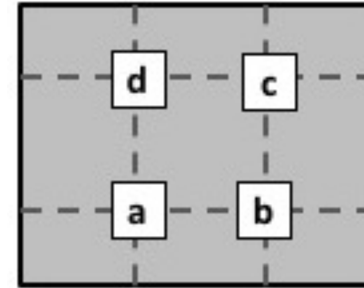
Group Representation
000000000010→0x02

Hotspot to Group Selection Mapper

- Scans non-empty windows in layout and generates forbidden selections
- Example



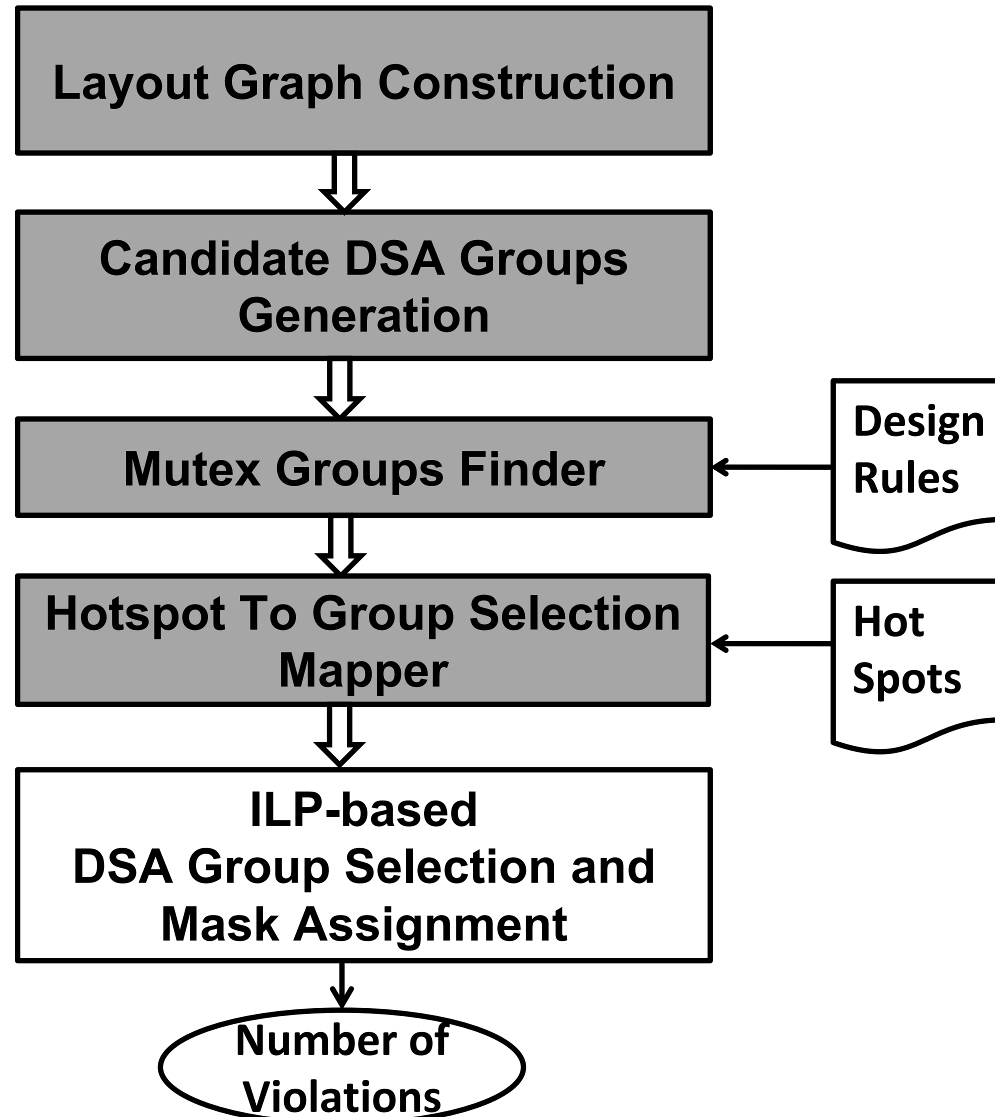
Hotspot



Layout Window

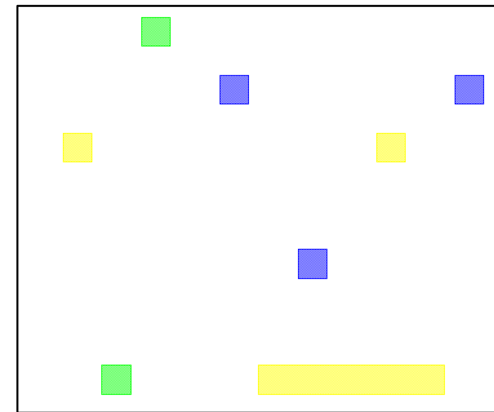
  – Hotspot will occur if the following combination occurs on the same mask:
    - **On Groups**: g{a,b}
    - **Off Groups**: g{b,c}, g{c,d}, g{a,d}
    - **Absent singletons**: c
- O(n)

Flow of the Framework



Integer Linear Program (ILP) Formulation

- Each graph component solved independently
  - Multiple threads
- **Optimal**
- Performs **DSA group selection** and **Mask assignment**
- **Cost Function:** minimize # conflicts
- Constraints:
  - Graph edge→ different mask or same group if possible
  - MUTEX groups constraints
  - Hotspot prevention constraints
  - Unidirectional group constraints



MINIMUM COST TECHNOLOGY FIX

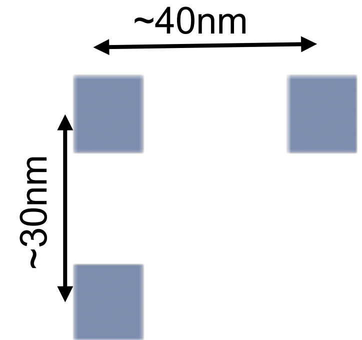
Minimum Cost Technology Fix

- ILP is solved to find the min-cost change for a design-friendly design
  - Costs are input to the framework
- Some of the allowed changes:
  - Decreasing ***min_pitch_same_mask***→ additional resolution enhancement cost
  - Decreasing ***min_pitch_diff_mask***→ cost of better overlay control
  - Increasing ***max_dsa_pitch*** and/or ***maxG***→resolution enhancement and BCP optimization
  - Removing **specific hotspot** → cost of design change or patterning change
  - Using an **alternative grouping checker**→ cost of different patterning scheme plus BCP optimization

CASE STUDIES

Test cases

- Macros placed and routed using a **projected 7nm library**
- Scaled down by 0.75 ➔ **5nm layouts**
- **Via1**
  - **dimensions**:
  - # vias: ~90K

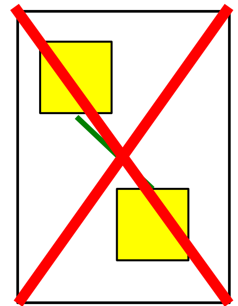


Test cases

- **Block Copolymer**
  - Natural pitch (also min pitch): 30nm
  - Maximum Groupable Pitch: 51nm
- **Min pitch** in 193i: 90nm
- **Min pitch** in EUV: 40nm
- Runtime
  - Design-friendliness metric: ≤11 minutes
  - Min-cost technology change: ≤ 4 hours

Case Study 1: Single Patterning EUV +long templates vs. Triple Patterning 193i + short templates

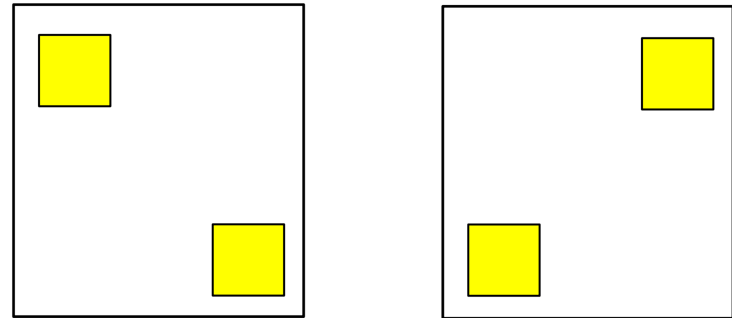
- Objective: Can we use EUV instead of Triple Patterning with 193i?
- **EUV** setup:
  - Non-manhattan (diagonal) groups disallowed
  - Max group size: 7
- **193i** setup:
  - Only collinear and manhattan groups
  - Max group size: 3



Test case	Num Vias	Num Violations EUV	Num Violations EUV Non manhattan	Num Violations TP+193i
aes	98896	134	0	0
mips	86939	186	0	0
usb	99366	152	0	0

Case Study 1: Single Patterning EUV +long templates vs. Triple Patterning 193i + short templates

- Objective: Can we use EUV instead of Triple Patterning with 193i? **Not without non-manhattan templates**
- Failing topologies:



- **Min Cost Technology Change:**
  - Reduce *EUV pitch* to 35 nm (instead of 40nm)

Case Study 2:193i With Uni-directional templates only

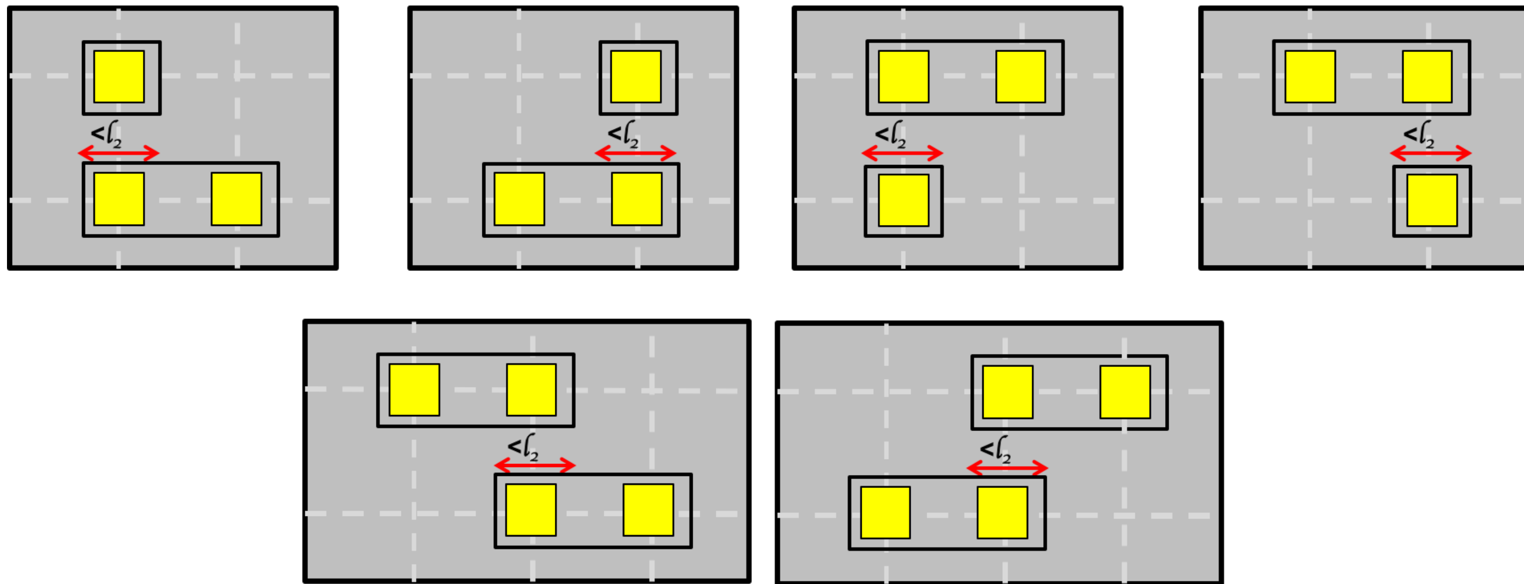
YES

- Objective: If each mask has **unidirectional** templates (either vertical or horizontal), is it still design-friendly?
- Setup:
  - Triple Patterning with 193i
  - **Two masks** are **Horizontal** and **one** is **vertical**

Test case	Num Vias	Num Violations birectional	Num Violations unidirectional
aes	98896	0	0
mips	98896	0	0
usb	99366	0	0

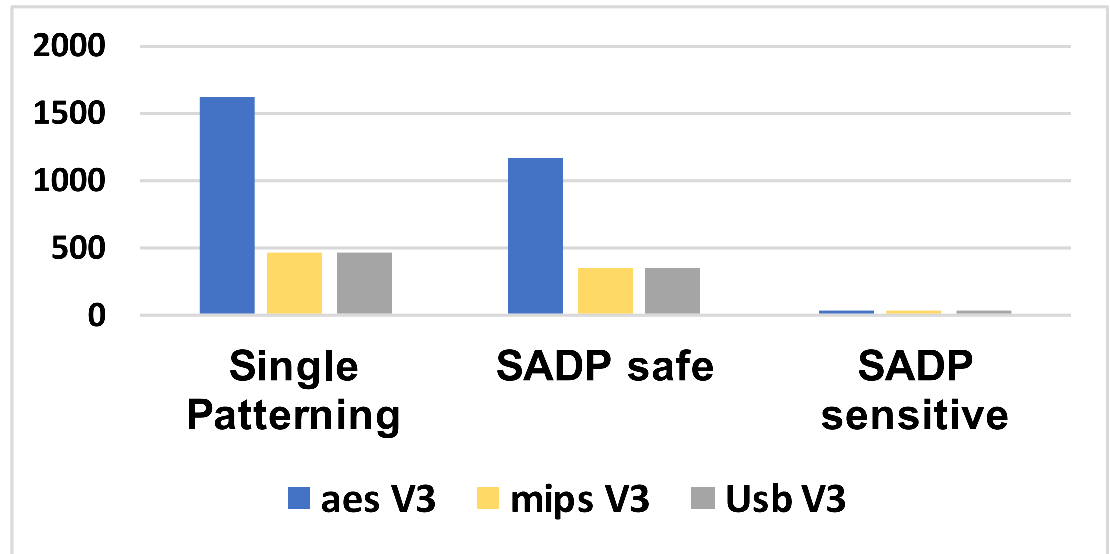
Case Study 3: Self-Aligned Double Patterning

- Objective: Can we use SADP to print templates for DSA? What if sensitive trim edges are allowed?
- Performed using hotspots
  - SADP-friendly DR from Xu et al.ISPD'14 represented as **Hotspots**
- **Min Off-track overlap rule:**



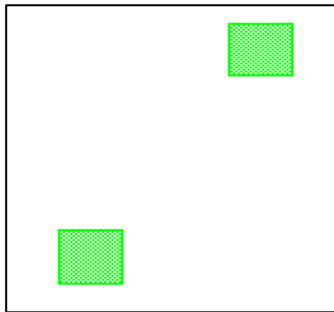
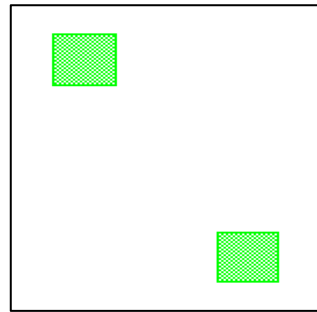
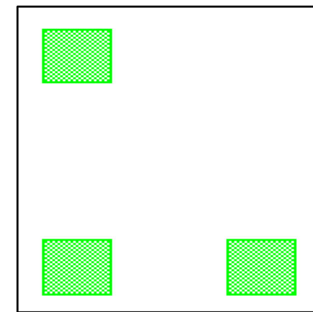
Case Study 3: Self-Aligned Double Patterning

- Setup:
  - DSA Range: 33-35nm
    - Tight because not peanut-shaped templates. Rect. Templates
  - On V3 layer

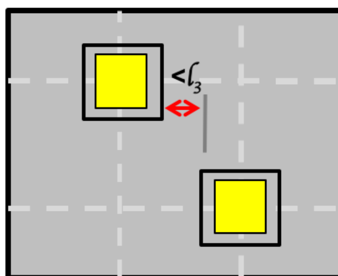
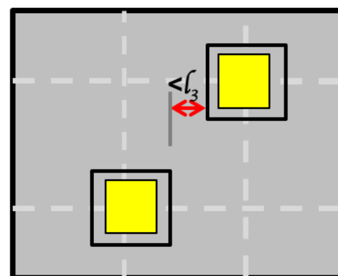
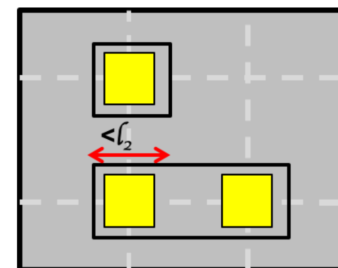


Case Study 3: Self-Aligned Double Patterning

- Samples of Violations
  - Snippets

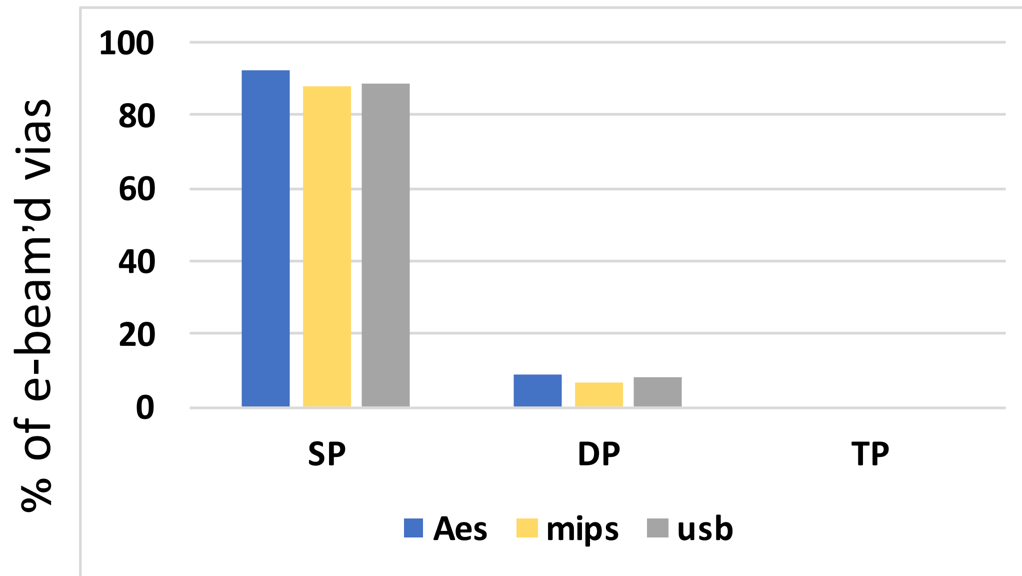
  - Resulting hotspots

- **Min cost technology change**
  - Remove hotspots→ SADP-aware design needed

Case Study 4: 193i + E-beam

- 193i to print templates → e-beam to print templates with violations
- Will it hurt throughput?
- Percentage of e-beam'd vias:



Conclusion

- Proposed a DSA pathfinding framework for vias (DSA_pathfind)
  - Available for download at: http://nanocad.ee.ucla.edu/Main/DownloadForm
- DSA_pathfind performs **optimal** evaluation of DSA-based technologies.
- Showed case studies involving multiple exposures of 193i, EUV, SADP and E-beam.

QUESTIONS