A Novel Methodology for Triple/Multiple-Patterning Layout Decomposition

Rani S. Ghaida[1], Kanak B. Agarwal[2], Lars W. Liebmann[3], Sani R. Nassif[2], Puneet Gupta[1]
[1] UCLA, Electrical Engineering Dept.
[2] IBM Corp., Austin Research Lab
[3] IBM Corp., Semiconductor Research & Development Center
{rani, puneet}@ee.ucla.edu {kba, lliebman,nassif}@us.ibm.com

ABSTRACT

Double patterning (DP) in a *litho-etch-litho-etch* (LELE) process is an attractive technique to scale the K_1 factor below 0.25. For dense bidirectional layers such as the first metal layer (M1), however, density scaling with LELE suffers from poor tip-to-tip (T2T) and tip-to-side (T2S) spacing. As a result, *triple-patterning* (TP) in a LELELE process has emerged as a strong alternative. Because of the use of a third exposure/etch, LELELE can achieve good T2T and T2S scaling as well as improved pitch scaling over LELE in case further scaling is needed. TP layout decomposition, a.k.a. TP coloring, is much more challenging than DP layout decomposition. One of the biggest complexities of TP decomposition is that a stitch can be between different two-mask combinations (i.e. first/second, first/third, second/third) and, consequently, stitches are color-dependent and candidate stitch locations can be determined only during/after coloring. In this paper, we offer a novel methodology for TP layout decomposition. Rather than simplifying the TP stitching problem by using DP candidate stitches only (as in previous works), the methodology leverages TP stitching capability by considering additional candidate stitch locations to give coloring higher flexibility to resolve decomposition conflicts. To deal with TP coloring complexity, the methodology employs multiple DP coloring steps, which leverages existing infrastructure developed for DP layout decomposition. The method was used to decompose bidirectional M1 and M2 layouts at 45nm, 32nm, 22nm, and 14nm nodes. For reasonably dense layouts, the method achieves coloring solutions with no conflicts (or a reasonable number of conflicts solvable with manual legalization). For very dense and irregular M1 layouts, however, the method was unable to reach a conflict-free solution and a large number of conflicts was observed. Hence, layout simplifications for the M1 layer may be unavoidable to enable TP for the M1 layer. Although we apply the method for TP, the method is more general and can be applied for multiple patterning with any number of masks.

1. INTRODUCTION

Delay in the deployment of EUV for volume manufacturing has left the semiconductor industry with no choice but to adopt *double patterning* (DP) to continue the scaling of technology. The *litho-etch-litho-etch* (LELE) process is one of the most favorable processes for DP. The two widely-accepted flavors of DPL, *pitch-split double-patterning* (PS-DP) in a *litho-etch-litho-etch* (LELE) process and *self-aligned double patterning* (SADP), have limitations that may hinder their application at sub-20nm process nodes. On one hand, PS-DP typically results in a large number of coloring conflicts (i.e. spacing violations after layout decomposition) that render the layout impossible to manufacture without making costly layout changes. On the other hand, SADP imposes near-grating layout making it unsuited for highly bidirectional layouts.

These limitations of DP technologies and the need for additional pitch relaxation has made *triple-patterning* (TP), in a LELELE process, a strong candidate solution to enable dense bidirectional metal layers with the least restrictions.

1.1 Complexity of TP Layout Decomposition

As all DP technologies, TP requires the layout to be decomposed into different masks. In common practice, layout decomposition is converted into a graph coloring problem, where nodes represent layout polygons and edges represent same-color spacing violations. Layout decomposition is challenging for PS-DP (as well as SADP) and it is even more challenging for TPL. In comparison with DP decomposition, the complexity of TP decomposition is attributed to the following.

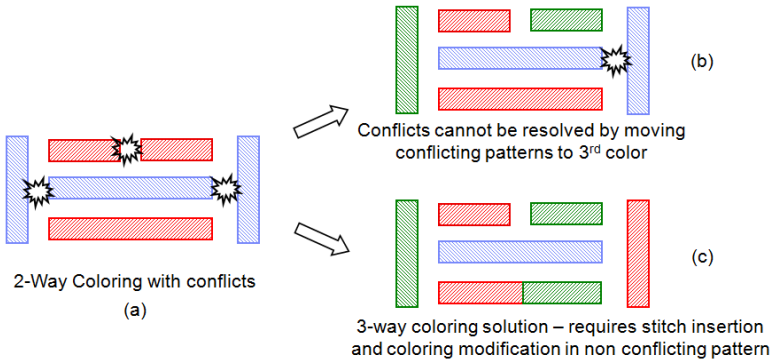


Figure 1: (a) Example layout decomposition with two colors showing conflicts, (b) TP layout decomposition with the ILP approach and the naive approach of using the third color to resolve conflicts, and (c) a conflict-free solution for TP layout decomposition.

1. Determining whether the layout is DP compatible (i.e. the graph is 2-colorable) can be done very efficiently (in polynomial time) by simply checking if the graph is free of odd cycles; whereas, determining whether the layout is TP compatible (i.e. the graph is 3-colorable) is an extremely hard problem for which there is no known efficient way to find a solution (classified as NP-complete problem in computational complexity theory). Moreover, in the 2-coloring problem, conflicts and their locations can be easily detected by identifying odd cycles in the conflict graph. In the 3-coloring problem, there are no existing methods for determining the number of conflicts and their locations.

2. In DP, candidate stitch locations can be determined prior to the actual coloring using projection. This enables coloring to consider all candidate stitch locations, which is crucial to achieve a solution with the minimum number of conflicts. In TP, however, a stitch can be between the first and second masks, the first and third masks, and the second and third masks. As a result, stitches are color-dependent and candidate stitch locations can be determined only after or during coloring.

1.2 Extending 2-Coloring to 3-Coloring

A naive extension of 2-coloring, layout decomposition for DP, to 3-coloring, layout decomposition for TP, is to start with a decomposition solution for DP and use the third color to resolve DP coloring conflicts. Although this approach is simple and does not require the development of new and sophisticated methods for TP layout decomposition, it may lead to a low-quality solution in terms of the number of conflicts. Consider the example in Figure 1. Figure 1(a) shows the initial DP coloring solution that contains conflicts; Figure 1(b) shows a TP coloring solution resulting from the naive approach and containing a conflict; and Figure 1(c) shows that a conflict-free TP coloring solution can be achieved with the use of a stitch.

Although ways for performing TP layout decomposition has been hinted at in some patent disclosures (e.g., [1]), the only complete previous work that covers TP layout decomposition for lines in LELELE process is the work of [2]. It suggests performing the TP layout decomposition by solving an integer linear program (ILP), which minimizes coloring conflicts as well as stitches. Solving the coloring problem with an ILP was shown to reach good solutions for DP [3–5] and the extension for TP is likely to reach good solutions for the 3-coloring problem as well. For design-level layout decomposition with large designs, solving the ILP is impractical because it requires a very long run-time. The work of [2] proposes an alternative solution, based on semidefinite programming, that is much faster than the ILP approach but leads to a larger number of coloring conflicts. The biggest limitation of the work of in [2] is that it uses candidate stitches that are only DP candidate stitches. Hence, many layouts can only be colored correctly for TP if TP stitches are used as in Figure 1)(b).

1.3 Overview of Our Approach

In this paper, we offer a novel methodology for TP layout decomposition that leverages TP stitching capability. Rather than simplifying the TP stitching problem by using DP candidate stitches only (as in previous works), the methodology

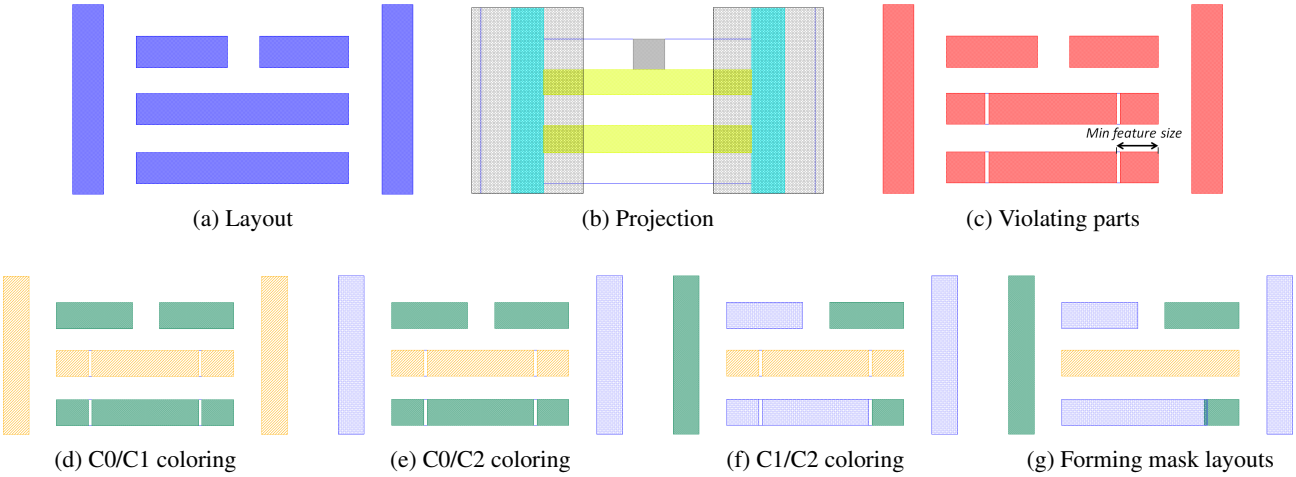


Figure 2: Example illustrating the application the different steps involved in our triple-patterning coloring methodology. In (b), T2S violations are expanded and the parts of the target layout that are covered after the expansion are the T2S violating parts. T2T and S2S violating parts are identified similarly.

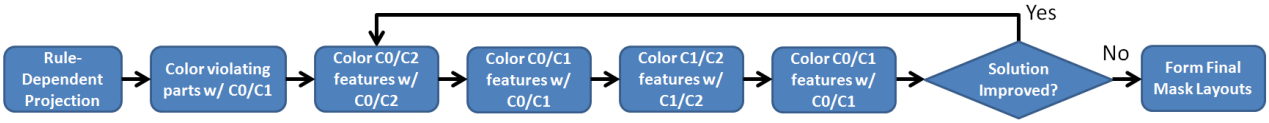


Figure 3: The flow for our the proposed TP coloring method that uses multiple steps of DP coloring.

considers additional TP candidate stitch locations to give coloring higher flexibility to resolve coloring conflicts. And, to deal with TP coloring complexity, the methodology employs multiple DP coloring steps, which leverages existing infrastructure developed for DP layout decomposition. We make the following contributions:

- We propose a method that performs TP layout decomposition that uses existing methodologies and algorithms developed for DP decomposition. Our TP decomposition method maximizes the use of stitching (among all three masks) to leverage TP stitching capability. The proposed method is also scalable and can be used to perform layout decomposition for multiple patterning with k-colors (with k being greater than or equal to 3) and can handle different values for tip-to-tip (T2T), tip-to-side (T2S), and side-to-side (S2S) same-color spacing rules.
- We test the method on different bidirectional layouts styles for 45nm, 32nm, 22nm, and 14nm technologies and report preliminary results.

2. DESCRIPTION OF THE PROPOSED METHODOLOGY FOR TP LAYOUT DECOMPOSITION

Our TP coloring method uses multiple steps of 2-coloring to achieve the decomposition of the layout into three colors. This allows the re-use of existing DP layout decomposition methods that are already developed and have reached maturity. For the DP layout decomposition, we follow the approach we described in a previous work [6]. The application of the different steps involved in our coloring method is illustrated by the example of Figure 2 and the different steps of the methodology are depicted in Figure 3. We use design rule-dependent projection as illustrated in Figure 4 to find all parts of the layout that have DP spacing violations with neighboring features and, then, we assign these violating parts to the two colors. In this way, candidate stitch locations are automatically defined as non-violating parts touching two or more violating parts. Stitches are then minimized by assigning these violating parts the same color. The TP coloring method involves a minimum of three DP coloring steps. First, we color the layout (violating parts only) with two colors C0 and C1. We then perform an additional coloring of the C0 layout using color C0 as well as the third color C2 to resolve conflicts on C0 (i.e. C0 to C0

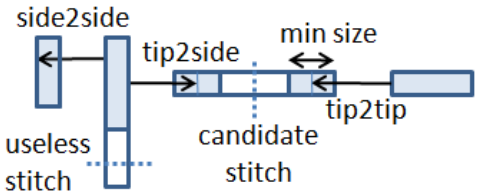
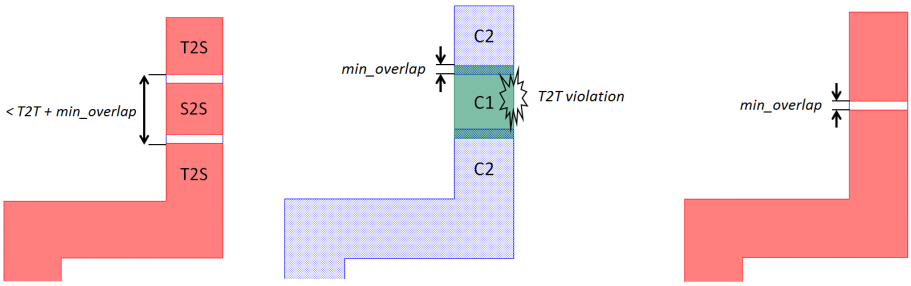


Figure 4: DR-dependent projection to identify violating parts and stitch locations. Violating parts are the blue features and non-violating parts are the clear features.



(a) (b) (c)

Figure 5: Illustrating example showing (a) candidate stitch at interface of S2S violating parts with other types of violating parts, (b) coloring problem that occurs with insertion of candidate stitch locations at interface, and (c) solving the problem by inserting a single stitch at center of S2S violating parts with length smaller than T2T (or T2S if larger) plus two times the minimum mask overlap length.

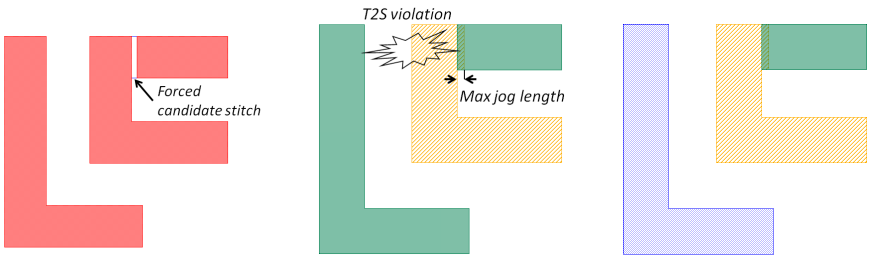
spacing violations). We perform a final coloring step for the combination of C1 and C2 features and using C1/C2 colors. Although the method can be used with any number of 2-coloring steps and any order of color combination at each step, we adopt the five 2-coloring steps in the order shown in Figure 3. We start with C0/C1 coloring and, whenever a new coloring with the third color is performed, we follow it with a new C0/C1 coloring step effectively enhancing the resolution of conflicts in the initial C0 and C1 layouts. This 2-coloring cycle could be repeated a number of times as long as the solution quality is improved or until a satisfactory solution is achieved.

It is important to note that, because we use multiple steps of 2-coloring to achieve layout decomposition for multiple patterning, our coloring method is scalable and can be used to perform layout decomposition for multiple patterning with k-colors with any k greater than or equal to 3.

2.1 Leveraging TP Stitching Capability

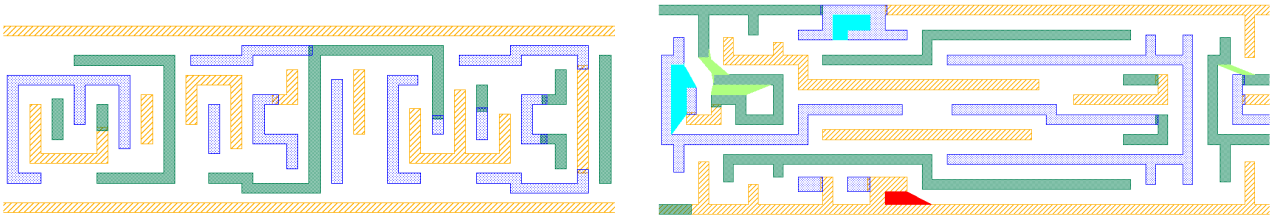
Although our approach is improved over the naive approach in that it resolves conflicts on C0 and C1 in separate steps, it can still fail to achieve a good-quality solution in many cases. Consider the example of Figure 1 again. The only way to reach a conflict-free coloring solution as in Figure 1(c) is by introducing a TP candidate stitch. Because locating candidate stitches with projection is performed prior to the actual coloring, no candidate stitch locations are found in this layout and coloring fails no matter what method is used. To avoid this problem, we perform projection for different spacing rules, T2T, T2S, and S2S, separately and introduce a candidate stitch location at the interface between purely S2S violating parts and the other types of violations (i.e. T2S and T2T violating parts). The intuition for inserting a stitch in S2S violating parts and not in other types of violations is that S2S violating parts are typically large and accommodate a split into multiple masks. Moreover, the only place where a candidate stitch is absolutely useless is when it is inserted at a location that is violating with two other shapes that are violating between one another; clearly, this occur much less often in the case of S2S violating parts than in the case of T2S or T2T violating parts.

When a S2S violating part is short (smaller than the T2T same-color spacing rule plus two times the minimum mask overlap length) and is between two (or more) violating parts from the other types of violations, a coloring conflict may occur in the final solution as illustrated in Figure 5. To prevent such conflicts, we insert a single candidate stitch location in the center of the S2S violating part instead of two candidate stitch locations at the two interface regions.



(a) (b) (c)

Figure 6: Illustrating example of the coloring of an U-shape violating part showing (a) forced candidate stitch insertion to separate the two segments of the U-shape, (b) the coloring problem that may occur once the coloring of violating parts and the mask layouts are formed, and (c) fixing the coloring with an extra coloring step post coloring of violating parts.



(a) (b)

Figure 7: Layout snippets of results of the proposed TP layout decomposition methodology when applied to standard-cell library designs at (a) 14nm with regular bidirectional M1 and (b) 22nm with more complex bidirectional M1.

For U-shapes violating parts (U-shapes on violating parts on the violating parts layer)where no stitches can be inserted with the method described earlier, we forcefully introduce a candidate stitch location at one of the U-shape segments, as illustrated in see Figure 6(a), so that the coloring tries to assign the two segments different colors. After the coloring of violating parts is complete and the mask layouts are formed, a coloring violation may occur between one of the U-shape segments and the neighboring features as illustrated in Figure 6(b). This can occur because such violation cannot be detected prior to coloring with edge-based projection performed using existing DRC tools. To reduce the occurrence of such violations, we introduce an extra coloring step after the features coloring is known with projection performed in each mask layout separately.

3. EXPERIMENTAL RESULTS

We test our methodology for TP layout decomposition on the M1 and M2 layouts of standard cell libraries as well as complete designs. The layouts varies in size and complexity: from complex bidirectional M1 layouts at 45nm and 22nm to more regular bidirectional M2 layouts at 32nm and M1 layouts at 14nm. In all experiments, we use a pitch relaxation factor close to 2X, a minimum mask overlap length of 10nm, and a minimum feature size equal to the minimum line width. We use three TP coloring cycles of the flow in Figure 3, which correspond to a total of thirteen 2-coloring steps, to enhance the coloring results in terms of the number of coloring conflicts.

Projection and identification of violating parts were implemented in Calibre SVRF [7] and 2-coloring steps were performed the DP layout decomposition algorithm of [6].

3.1 TP Layout Decomposition Results for 45, 32, 22, and 14nm Nodes

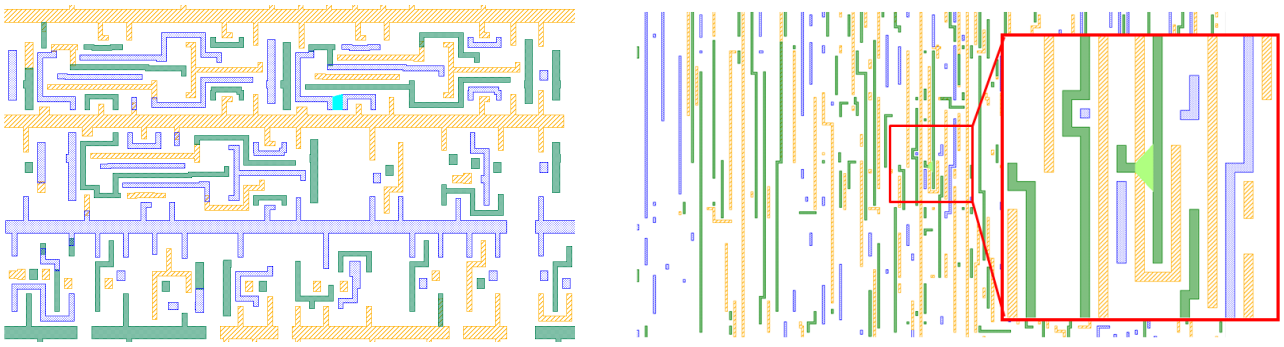
We tested the proposed decomposition methodology on the M1 layer of two standard-cell libraries: the first is a 14nm library of 22 cells with bidirectional but simple M1 layout and the second is a 22nm library with extremely dense and irregular M1 patterns in all cells (to maximize M1 pin access). For the 14nm library, the method achieved a conflict-free coloring solution; for the 22nm library, however, the method resulted in a large number of TP coloring conflicts. The

Table 1: Summary of results for the proposed TP coloring methodology when applied on library and full-design layouts at 45, 32, 22, and 14nm nodes.

Layout	# of Cells	Pitch Relaxation	# of Conflicts	# of Stitches
14nm Library	22	2X	0	33
22nm Library	108	1.9X	285	1,181
32nm M2 Design	26,000	2X	54	5,215
45nm M1 Design A	3,000	1.9X	177	842
45nm M1 Design B	10,000	1.9X	1,322	9,825

Table 2: Results comparison between TP and DP coloring.

Layout	# of TP Conflicts	# of DP Conflicts	# of TP Stitches	# of DP Stitches
14nm Library	0	39	33	8
22nm Library	285	1,100	1,181	520
32nm M2 Design	54	3,272	5,215	1,712
45nm M1 Design A	177	4,524	842	1,310
45nm M1 Design B	1,322	27,073	9,825	8,044



(a) (b)

Figure 8: Layout snippets of results of the proposed TP layout decomposition methodology when applied to full-design layouts at (a) 45nm with irregular bidirectional M1 and (b) 32nm with bidirectional but more regular M2.

results are summarized in Table 1 and layout snippets showing the level of the layouts complexity are shown in Figure 7. Note that the results correspond to a single layout per library where cell-layouts are abutted to form the complete layout.

We also test the coloring methodology on full-design layouts at 45 and 32nm nodes. At 45nm node, we decompose the M1 layer for TP in two designs one with 3,000 cells and the other with 10,000 cells. The M1 for both designs is highly irregular and are composed of cells with low as well as high density (unlike our test case for 22nm where all cells were very dense). The results, highlighted in Table 1, show a reasonable number of conflicts for the smaller design suggesting that fixing the layout with manual incremental coloring or redesign would be possible for small designs (e.g., macros with ¡ 3,000 cells); for large designs, however, fixing the layout seems intractable. It is important to note that many of the coloring conflicts are repeated in certain problematic cells; so, fixing the layouts of such cells can greatly reduce the overall number of conflicts. At 32nm node, we perform the layout decomposition for the M2 layer (i.e. first routing layer) of a 26,000-cells design. Even though the design is fairly large, the coloring resulted in 54 conflicts only. Fixing such a limited number of conflicts is tractable with rip-up and re-route or manual incremental coloring or redesign. Figure 8 shows the level of complexity of the 45 and 32nm layouts as well as an example coloring conflict in each case.

When inspecting the final colored layouts, we observed that a considerable portion of the conflicts were caused by newly created tips at stitch locations once the final mask layouts are formed as illustrated in Figure 9. Although this problem occurs in DP layout decomposition when the T2T/T2S rules are lareger than the S2S rule, it occurs more frequently in TP layout decomposition because of the use of three masks and the problem may occur even when the rules have the same value because of the stitching at S2S violating parts. In future work, we plan to address this issue by modifying the exact

Table 3: Summary of results for the proposed TP coloring methodology when applied on library and full-design layouts at 45, 32, and 22nm nodes with pushed T2T and T2S same-color rules from 3X to 2X the minimum spacing.

Layout	Original # of Conflicts	# of Conflicts w/ Pushed Rules	Original # of Stitches	# of Stitches w/ Pushed Rules
22nm Library	285	207	1,181	1,143
32nm M2 Design	54	50	5,215	5,566
45nm M1 Design A	177	92	842	809
45nm M1 Design B	1,322	465	9,825	8,918

Table 4: TP coloring results with and without employing the TP stitching method (i.e., insertion of candidate stitches in S2S violating parts).

Layout	Original # of Conflicts	# of Conflicts w/o TP stitching method	Original # of Stitches	# of Stitches w/o TP stitching method
14nm Library	0	0	33	0
22nm Library	285	410	1,181	695
32nm M2 Design	54	66	5,215	3,135
45nm M1 Design A	177	366	842	548
45nm M1 Design B	1,322	3,144	9,825	4,044

Table 5: Run-time in real time of the proposed TP coloring methodology including projection, graph constructions, and all 2-coloring steps (twelve steps).

Layout	# of Cells	Pitch Relaxation	Run-time
14nm Library	22	2X	1min 30s
22nm Library	108	1.9X	2min 20s
32nm M2 Design	26,000	2X	7min 10s
45nm M1 Design A	3,000	1.9X	4min 16s
45nm M1 Design B	10,000	1.9X	28min

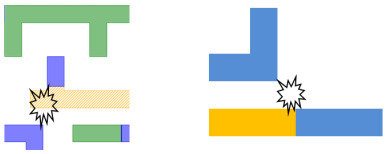


Figure 9: Coloring conflicts that may occur due to newly created tips.

locations of candidate stitches to avoid such conflicts.

3.2 Comparison with DP Layout Decomposition

We compare the TP coloring results to DP coloring for all test cases. As Table 2 shows, the number of conflicts with TP coloring is one to two orders of magnitude smaller than with DP coloring. The number of stitches is considerably larger in TP coloring for most cases, however. This is attributed to the facts that our TP coloring methodology makes use of TP stitching capability and that the methodology does not minimize the number of stitches globally between different coloring steps (while the DP coloring minimizes the stitching in the single coloring step).

3.3 Pushing T2S and T2T Same-Color Rules

The results in Table 1 are for the case where the T2T and T2S same-color spacing rules are equal to the S2S same-color spacing, which is roughly 3X the minimum spacing in the layout. T2T and T2S could be possibly pushed, however. Therefore, we repeat the experiments with pushed T2T and T2S same-color rules to 2X the minimum spacing. The results, reported in Table 3, show that pushing the T2T and T2S same-color rules greatly reduces the number of TP coloring conflicts but does not solve the problem entirely.

3.4 Effects of Using the Proposed TP Stitching Method

To quantify the impact of using the proposed TP stitching method (i.e., candidate stitch insertion in S2S violating parts), we compare the results with the case when this method is not used and candidate stitches for TP coloring are candidate stitches for DP. The results summarized in Table 4 indicate that the TP stitching method is effective in reducing the number of coloring conflicts (except for the 14nm layout where conflict-free solutions are achieved in both cases).

3.5 Run-time Results

Even though the proposed 3-coloring methodology involves several 2-coloring steps (twelve 2-coloring steps), the run-time is not a concern. Table 5 reports the run-time of the complete process of projection, graph constructions, and all 2-coloring steps for all test cases.

4. CONCLUSIONS

We proposed a novel methodology for TP layout decomposition that employs existing 2-coloring infrastructures available for DP to perform 3-coloring. Rather than simplifying the TP stitching problem by using DP candidate stitches only, the methodology leverages TP stitching capability by considering additional candidate stitch locations to enhance the coloring efficiency. The method was used to decompose M1 layouts in standard-cell libraries; for simple M1 layouts at 14nm, the method achieved conflict-free solutions; for very dense M1 layouts at 22nm, however, the method resulted in a large number of conflicts. The method was also used to perform full-design layout decomposition of M1 and M2 layers; results show a reasonable number of TP coloring conflicts on the M1 layer in small designs and a limited number of conflicts on the M2 layer in fairly large M2 layouts. Hence, TP has the capability of achieving violation-free coloring for bidirectional routing layers as well as irregular M1 layer in small layouts; TP is unlikely to achieve legal coloring for extremely dense and irregular M1 in large designs, however, and some layout simplification may be unavoidable. In future work, we plan to address the issue with newly created tips described earlier and minimize TP stitches globally across the multiple 2-coloring steps.

REFERENCES

[1] Socha, B., "Method, program product and apparatus for performing a model based coloring process for geometry decomposition for use in a multiple exposure process," (2010).

[2] Yu, B., Yuany, K., Zhang, B., Ding, D., and Pan, D. Z., "Layout decomposition for triple patterning lithography," in [*Intl. Conf. on Computer-Aided Design*], 1–8 (2011).

[3] Kahng, A. B., Park, C.-H., Xu, X., and Yao, H., "Layout decomposition approaches for double patterning lithography," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* **29**(6), 939–952 (2010).

[4] Yuan, K., Yang, J.-S., and Pan, D. Z., "Double patterning layout decomposition for simultaneous conflict and stitch minimization," in [*Intl. Symp. on Physical Design*], 107–114 (2009).

[5] Yang, J.-S., Lu, K., Cho, M., Yuan, K., and Pan, D. Z., "A new graph theoretic, multi-objective layout decomposition framework for double patterning lithography," in [*IEEE Asian and South Pacific Design Automation Conference*], 637–644 (2010).

[6] Ghaida, R. S., Agarwal, K. B., Nassif, S. R., Yuan, X., Liebmann, L. W., and Gupta, P., "A framework for double patterning-enabled design," in [*Intl. Conf. on Computer-Aided Design*], 1–8 (2011).

[7] "Calibre standard verification rule format manual v2009."