Design-of-Experiments Based Design Rule Optimization

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ABSTRACT

Design rules (DRs) are the primary abstraction between design and manufacturing. The optimization of DRs to achieve the correct tradeoff between scaling and yield is a key step in developing a new technology node. In this work we propose a design-of-experiments based framework to optimize DRs, where layouts are generated for different DR values using compaction. By analyzing the impact of DRs on layout scaling, we propose a novel Boolean minimization based approach to reduce the number of layouts that need to be generated through compaction. This methodology provides an automated approach to analyze several DRs simultaneously and discover area-critical DRs and DR interactions. We apply this methodology to middle-of-line (MOL) and Metal1 layer design rules for a commercial $20nm$ process. Our methodology results in $10 - 10^5\times$ reduction in the number of layouts that need to be generated through compaction, and demonstrates the impact of MOL and Metal1 DRs on the area of some standard cell layouts.

1. INTRODUCTION

The resolution limits of $193nm$ lithography coupled with the delay of production ready Extreme Ultraviolet (EUV) lithography has necessitated the need for several process innovations to ensure scaling. This includes multiple patterning, use of restricted DRs and the introduction of local interconnect layers. These changes have had a significant impact not just on the manufacturing process but on circuit design as well. Design rules (DRs) provide a seamless abstraction of the capabilities of the manufacturing process to circuit designers in the form of geometric constraints on circuit layout shapes. Simultaneously, DRs serve as a target that the foundry needs to meet by tuning process parameters. The number and complexity of design rules has been growing rapidly with each technology node, with page count of design rule manuals increasing by $2\times$ with each technology node.[8] Apart from significant impact on chip area and manufacturing yield, these DRs affect electrical metrics like power, delay and crosstalk. DRs also influence the behaviour of placement and routing tools during physical design.

Design Rule optimization is the process of determining the precise DR values for a new technology node. It is an extremely critical part of ramping up a new technology node and it typically involves several iterations between the foundry and early technology adopters. On the foundry side, DR values are determined by evaluating critical test structures, either through process simulation or test wafer runs. This approach allows the foundry to analyze each rule separately and determine the resolution limits of the process. On the other hand, circuit designers generate standard cell layouts, either manually or through automated layout generation tools such as Progenesis[1] to evaluate the design impact of various design rules. But optimizing hundreds of DRs simultaneoully for several different layout patterns is a computationally intractable problem. As a result, DR optimization is a slow and ad-hoc process. Hence, there is a strong need to develop a systematic and automated approach to optimize DRs.

Several previous works have looked at methods for design rule optimization. Most approaches focus on lithography simulation based analysis to explore design rules. For example, Zhang et. al.[10] analyzed test structures to determine the minimum resolvable design rule values by simulating test structures. Similarly, Chang et. al.[5] explored metal layers DRs by evaluating both parametrized test structures and real layout features using an inverse lithography tool. Ho et. al.,[7] on the other hand, performed full chip lithography simulation to first find hot-spots which are then used to improve the design rule set. Lithography simulation based approaches cited above do not evaluate the design impact of DR values, either with respect to their impact on chip area or any electrical metric like performance, power and signal integrity. Capodieci et. al.[4] suggested a more comprehensive approach based on automated generation of standard cell layouts that analyzes the impact of DRs on layout area, manufacturing yield, performance and even mask cost. Unfortunately, the slow and cumbersome nature of layout generation limits the approach to analyzing only one rule at a time for a few critical DRs. Ghaida et. al.[6]

proposed a novel approach to evaluate several DRs and layout topologies by developing a fast layout and yield estimation. But the approach only "estimates" layouts and hence suffers from limited accuracy. This prevents the usage of such a framework to determine precise DR values.

In light of the limitations of previous approaches to co-optimize several design rules simultaneously with respect to both design and process metrics, we propose a systematic and hierarchical framework to co-optimize DRs illustrated in Figure 1. This framework first explores several different DR rules and layout styles using a fast layout and yield estimator to find the some good candidate solutions. For each of these candidate DR sets and layout styles, standard cell layouts are generated either through automatic layout generation tools or through manual layout design. This is the slowest step of the proposed framework. Finally, for each of these standard cell layouts, layout compaction can be used to perturb DR values and analyze the impact on compacted layouts. This paper focuses on the last step of the DR optimization framework in

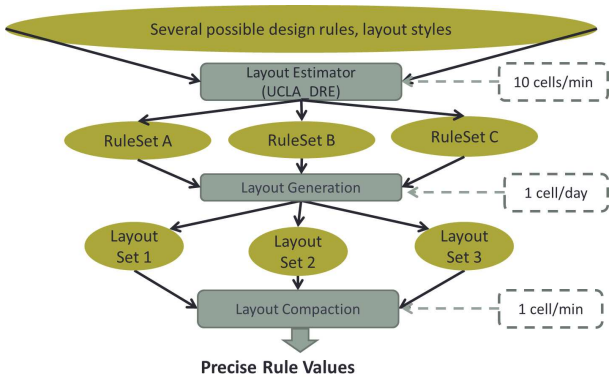

Figure 1. Hierarchical framework for design rule optimization.

Figure 1, compaction-driven fine-tuning of DRs. More specifically, we focus on the area impact of DRs. The description of our compaction-based method is covered in Section 2. To reduce the number of layouts that need to be generated for this compaction-driven DR optimization, we propose a novel Boolean minimization based experiment reduction methodology in Section 3. The methodology is applied to a commercial $20nm$ DR set in Section 4. Finally, we conclude this work in Section 4.

2. COMPACTION-DRIVEN DESIGN RULE OPTIMIZATION

Layout compaction or migration is the process of perturbing an existing layout to achieve the minimum possible area while adhering to the set of input design rules. A layout compaction tool allows a convenient framework to explore DRs. Starting with a DRC-clean input layout, we can perturb a chosen set of DR values and generate minimum area output layouts which are DRC-clean with respect to the perturbed design rule values. This framework is illustrated in Figure 2. These output layouts, which we shall refer to as variant layouts, can then be analyzed to evaluate the impact of DR value changes on design and process metrics. In this work, we only analyze the impact of DRs on area.

A compaction based approach to explore DRs, using the framework illustrated in Figure 2, has several advantages. It allows us to analyze the impact on relevant metrics when multiple DR values are changed simultaneously. Hence DR interactions can be accurately estimated. Since it only moves layout shapes, it is significantly faster than layout generation. The primary drawback of this approach is that it is useful only when the change in DR values is not very large. This is because in such a scenario, a different layout topology may be required to achieve minimum area, a solution that compaction cannot discover.

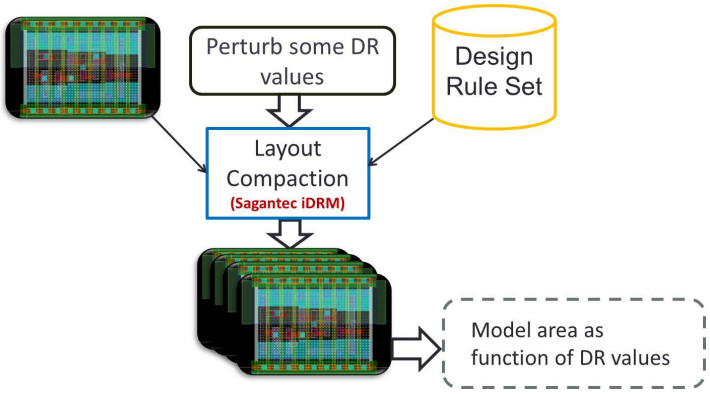

Figure 2. Design rule optimization using layout compaction.

3. EXPERIMENT REDUCTION METHODOLOGY

Consider a case where we need to analyze a set of k design rules $(d_1, d_2, \ldots d_k)$ each with m different levels using the compaction based approach of the previous section. If we were to use a naive approach, we would need to generate m^k variant layouts. Even for analyzing just 10 design rules each with 5 levels, we would need to generate 5^{10} variant layouts through compaction, which is clearly intractable. In order to reduce the intractable number of "experiments" (variant layout generation and analysis) that need to be performed in case of a naive compaction based approach, we propose a novel experiment reduction methodology in this section. A brief overview of the various steps of our experiment reduction methodology are as follows:

1. Choose a set of k DRs, $d_1, d_2, \ldots d_k$ that need to be optimized simultaneously.
2. *Two-level Experiment:* Considering only two values per DR, d_i^{min} and d_i^{max}, 2^k variant layouts are generated using compaction, Area of each of these variant layout is computed.
3. *Boolean Minimization:* Find minimal Boolean expression for each unique area value, which prunes out DRs and their interaction terms that do not affect area.
4. *Multi-level Experiment:* Perform a fine-grained analysis of the area-critical DRs and DR interaction terms only to model area as a function of DRs.

In the following we describe each of these steps in detail, with formal quantification of the reduction in experiment size achieved as a result of our approach.

3.1 Two-level Experiment

Once a set of DRs are chosen for analysis, only two discrete values are considered for each DR, d_i^{min} and d_i^{max} in this step. The lower value d_i^{min} is taken as the default value in the design rule manual (DRM). The higher value, d_i^{max} is taken as 20% higher than the DRM value. The choice of 20% as the upper limit of DR value change is arbitrary. A large DR value change is unacceptable since compaction based DR optimization makes sense only for small DR value changes, as pointed out earlier in Section 2. Very small DR value changes, on the other hand, may leave little room for DR value optimization. We, therefore, generate 2^k variant layouts for each input layout, corresponding to all the different combinations of DR values. The area of each of these variant layouts is measured. The result of this two-level experiment can be represented as a table with $k+1$ columns and 2^k rows. The first k columns consist of DR values for the k DRs being analyzed and the last column is the area of the corresponding variant layout.

3.2 Boolean Minimization

The key observation underlying the method of Boolean minimization for reducing experiment size, using just the two-level experiment, is that the relevant metric, area, is a monotonic function of DR values. This implies that whenever any DR value is increased, the layout area either increases or remains unchanged. This monotonicity allows us to prune out DRs and their interaction terms that do not affect area with only a two-level experiment, by using Boolean minimization.

The first step to analyze the $2^k \times (k+1)$ tabular result obtained from the two-level experiment in Section 3.1 is to abstract all the DRs as Boolean variables, i.e. for each DR d_i, i.e. replace d_i^{min} by FALSE and d_i^{max} by TRUE. Then find the number of distinct area values among all the 2^k experiment results. Suppose T unique area values $A_1, A_2 \ldots A_T$ are obtained. The two-level experiment table is then scanned to find all the variant layouts which have the same area value A_t. We can then write a Sum-of-Products form Boolean expression for A_t with each DR d_i represented as a Boolean variable b_i. This Boolean expression is then minimized to obtain a minimal Boolean expression corresponding to A_t. A sample Boolean expressions is illustrated in Equation 1. This procedure is repeated for all the area values $A_1, A_2 \ldots A_T$ to get T minimal Boolean expressions corresponding to each unique area value.

$$A_t \rightarrow \bar{b_1}\bar{b_2}\ldots\bar{b_{k_1}}b_{k_1+1}\ldots b_{k_2} + more \quad minterms \tag{1}$$

The set of T minimal Boolean expressions we obtain for each unique area value of the two-level experiment provides a compact and insightful overview of how design rules affect layout area. It also provides a precise means of determining which DRs or DR interaction terms actually impact area. For example, suppose we analyze a set of three DRs d_1, d_2 and d_3. A sample solution set with three unique area values A_1, A_2 and A_3 along with the Boolean expression before and after minimization is shown in Equations 2-4. The minimized Boolean expressions here imply that DR b_1 does not affect area, and DR b_3 is area-critical only if DR r_2 has value greater than d_2^{min}.

$$A_1 \rightarrow \bar{b_1}\bar{b_2}\bar{b_3} + \bar{b_1}\bar{b_2}b_3 + b_1\bar{b_2}\bar{b_3} + b_1\bar{b_2}b_3 \rightarrow \bar{b_2} \tag{2}$$

$$A_2 \rightarrow \bar{b_1}b_2\bar{b_3} + b_1b_2\bar{b_3} \rightarrow b_2\bar{b_3} \tag{3}$$

$$A_3 \rightarrow \bar{b_1}b_2b_3 + b_1b_2b_3 \rightarrow b_2b_3 \tag{4}$$

Similarly, for a general minterm as shown in Equation 1, $r_1 = (k - k_2)$ DRs do not matter, i.e any value (low or high) of these DRs does not change the layout area. This assumption is valid due to the monotonic nature of area with respect to DRs. Hence, all the following types of cases can be eliminated from the complete experiment: $(d_1, \ldots, d_{k_1})$ at minimum level $(d_{k_1+1}, \ldots, d_{k_2})$ at maximum level and any non-minimum value for the rest of the variables. Hence, a total of $m^{r_1} - 1$ cases are eliminated from the multi-level experiment. If there are a total of n minterms corresponding to different area values (each area value can have multiple minterms) and minterms have $r_1, r_2 \ldots r_n$ don't care variables, then the total number of experiments that need to be run is shown in Equation 5 and 6.

$$numExpTwoLevel = 2^k \tag{5}$$

$$numExpMultiLevel = (m^k - m^{r_1} - m^{r_2} - \ldots - m^{r_n} + n - 2^k) \tag{6}$$

An important observation here is that some of the DRs will not be present in any of the T Boolean expressions. This means that such DRs are non-critical for scaling, i.e. changing these increasing these DR values by 20% will have no impact on the area of the layout under consideration. The reduction in number of experiments achieved by not perturbing such non-critical DRs is already accounted for in Equation 6. Clearly, a significant advantage of the Boolean minimization approach is that it provides a quick visual interpretation of DRs that actually matter.

3.3 Multi-level Experiment

The last step of our approach is to generate variant layouts only for the critical DRs and DR interaction terms as determined by the Boolean minimization approach discussed in the previous section. But instead of considering only two levels for these DR terms, multiple levels ranging from d_i^{min} to d_i^{max} are considered for each DR, with the minimum allowable step size. The minimum allowable step size is typically the grid size of the layout, which in our experiments is $1nm$. Once variant layouts are generated for the relevant cases with a grid-size granularity, layout area can be modeled as a function of DR values. Conventional regression based fitting could be employed, but it is unlikely to work well due to the discrete

nature of change in area with DR values. If the number of experiments that need to be performed in the multi-level stage is not too large, a look-up table based model could be used.

Note that in the worst case scenario $r_1 = r_2 = \ldots r_n = 0$. As a result, no reduction in experiment size is obtained from this approach and a total of m^k experiments will have to be run. Hence, this approach does not guarantee reduction in experiments but relies on the fact that for most layouts, only a small subset of DRs and interactions actually affect layout area.

3.4 Further Experiment Reduction: Ignoring Neighborhood Interactions

In addition to the limitation that the Boolean minimization based approach does not guarantee experiment reduction, this approach cannot handle an arbitrarily large number of DRs. This is because 2^k variant layouts need to be generated in the two-level experiment initially, which increases exponentially as the number of DRs, k, increases. In order to reduce the number of experiments in the two-level experiment, we need to make simplifying assumptions. In this work, we assume that only the interaction of DRs of non-neighboring layers can be ignored. Suppose we have l layers, $L_1, L_2, \ldots L_l$ each with $k_{L_1}, k_{L_2}, \ldots k_{L_l}$ rules where L_1 and L_2 are neighbors, L_2 and L_3 are neighbors and so on. Since only neighboring layers interact, we can construct separate binary factorial experiments for each set of interacting rules. Then the reduction achieved by splitting a single large factorial experiment to multiple smaller factorial experiments is as shown in Equation 7.

$$\Delta Runs = 2^{k_{L_1}+k_{L_2}+\ldots k_{L_l}} - (2^{k_{L_1}+k_{L_2}} + 2^{k_{L_2}+k_{L_3}} + \ldots 2^{k_{L_{l-1}}+k_{L_l}}) \quad (7)$$

4. EXPERIMENTAL RESULTS

Sagantec iDRM[3] is used as the compaction engine of our DR optimization framework. The tool allows us to generate DRC-clean variant layouts when DR values are perturbed through layout compaction. The methodology was evaluated for $20nm$ design rules which are currently under development at GlobalFoundries. A total of 16 DRs corresponding to local interconnect and Metal1 layers are perturbed to generate variant layouts using the compaction tool. In addition to the these perturbed DRs, 52 additional DRs corresponding to polysilicon, active, local interconnect, contact and Metal1 layers are coded into the compaction tool. These DRs are not perturbed during our analysis but are treated as constraints during compaction. Transistor sizes are kept fixed during compaction to prevent any performance impact. MOL and Metal1 layer DRs are chosen for analysis because these layers are undergoing significant changes at $20nm$. Local interconnect layers are being introduced at $20nm$, while Metal1 will be double patterned. Hence, analyzing the design impact of DRs of these layers is extremely critical for rule development.

Seven different standard cell layouts, which were DRC-clean with respect to rule values in the DRM, were analyzed using this methodology. The Boolean minimization was performed using an existing MATLAB implementation of Quine-McCluskey algorithm.[9] Area of variant layouts was computed using Mentor Calibre.[2] For analyzing the 16 DRs, 2^{16} variant layouts need to be generated for the two-level experiment. The experiment reduction method we proposed in Section 3.4 is used to reduce the number of experiments required (This simplification assumes that since MOL and Metal1 layers are not neighbors, their DRs do not interact.). Hence, the rule set to be analyzed is split into two groups: One group for MOL layers and another for Metal1 layer. Note that DRs corresponding to the contact layer, which connects MOL and Metal1, are included in both these groups. We shall present results for these two groups of DRs separately.

4.1 Middle-of-Line DR Analysis

A total of 9 DRs corresponding to local interconnect and contact layers are considered here. Without our experiment reduction methodology, each of these DRs must be perturbed in steps of $1nm$ (grid size) to accurately model area as a function of these DR values. A total of 3×10^7 variant layouts per standard cell layout would be required to perform this analysis. Using our experiment reduction approach, only 512 variant layouts need to be generated for the two level experiment for each standard cell. These results are then analyzed using our Boolean minimization based approach. Let us observe the result after Boolean minimization for one standard cell, OAI22. After generating 512 variant layouts and computing the area of all the layouts, we found that there are 8 unique area values. Binning all the tabular entries for each area value and performing Boolean minimization, a minimal Boolean expression for each area value is obtained as shown in Equation 8-14, where the area values shown is normalized. From these equations, we can see that only three rules

Table 1. Summary of Boolean minimization for MOL layer DR analysis of 20nm standard cell layouts

Cell Name	# Critical Rules	Max. Area Increase (%)	# Multi-level Experiments Required
CKBF2	0	0	0
NAND2	2	1.1%	22
NOR2	2	1.4%	14
MUX21	2	1.7%	13
MUX22	2	0.7%	22
OAI22	3	7.8%	286
SDFFQ	0	0.0%	0

are area-critical, d_2, d_4 and d_9. Another observation from Equation 1 is that when $d_2 = d_2^{min}$ and $d_9 = d_9^{min}$, all cases where d_4 varies from d_4^{min} to d_4^{max} can be ignored without losing any accuracy in modeling area. With these reductions, perturbing each of these three critical rules in steps of $1nm$ from d^{min} to d^{max}, would require 286 variant layouts in the muli-level stage.

$$1.000 \rightarrow \bar{d_2}\bar{d_9} \tag{8}$$
$$1.020 \rightarrow \bar{d_2}\bar{d_4}d_9 \tag{9}$$
$$1.022 \rightarrow \bar{d_2}d_4d_9 \tag{10}$$
$$1.042 \rightarrow d_2\bar{d_4}\bar{d_9} \tag{11}$$
$$1.051 \rightarrow d_2d_4\bar{d_9} \tag{12}$$
$$1.069 \rightarrow d_2\bar{d_4}d_9 \tag{13}$$
$$1.079 \rightarrow d_2d_4d_9 \tag{14}$$

The results after Boolean minimization for all the standard cells are summarized in Table 1. For two standard cells, CKBF2 and SDFFQ, there is no impact on cell area for the two-level experiment. *This implies that increasing the DR value of all the* 9 *MOL rules considered by* 20% *will not increase their cell area.* For all the other standard cells that were analyzed, only $2-3$ DRs are area-critical. The number of experiments that need to be performed in the multi-level step are shown as well.

For the two-level experiment, area of a standard cell variant layout is maximum when all the 9 DRs that are perturbed have a value 20% higher than the default manual value. We report the percentage difference between the area of this variant layout and the nominal unperturbed layout and report it in Table 1. Notice that only one standard cell, OAI22, has a significant change in area during this analysis. Hence, we focus on this standard cell for the multi-level experiment. 286 more variant layouts are generated for the OAI22 standard cell, where relevant DR values are perturbed in steps of $1nm$.

The results for the multi-level experiment for OAI22 layout is summarized by the scatter plot in Figure 3, with area on the y-axis and sum of the three area-critical DRs on the x-axis. Since only 286 data-points are required to completely model area of the OAI22 cell as a function of the three area-critical DRs, a look-up table is used instead of any regression or machine learning based model.

The sum of DR rules can be considered as a rough metric that tracks the improvement in manufacturing yield with DR value change. With this approximation, we can plot the optimum design-process tradeoff using the look-up table based area model, as shown by the curve in Figure 3. For a full chip design with several different standard cells, a weighted sum of the area of different cells can be used, with weights assigned based on their usage in the design. In our case, since OAI22 is the only standard cell with a significant area change[1], the full chip design-process tradeoff curve would be a scaled version of this plot. Overall, these results show that for the set of standard cell layouts that we analyzed, MOL layer DRs do not affect scaling significantly. This implies that MOL DRs can be relaxed without any area penalty for all the standard cell layouts we considered (except OAI22). It also suggests that DRs that actually limit scaling actually lie in other critical layers that we have not analyzed so far, either front-end polysilicon and active layers, or Metal1.

[1]Less than 2% area change for 20% DR value change in all the other standard cells is insignificant and hence not modeled.

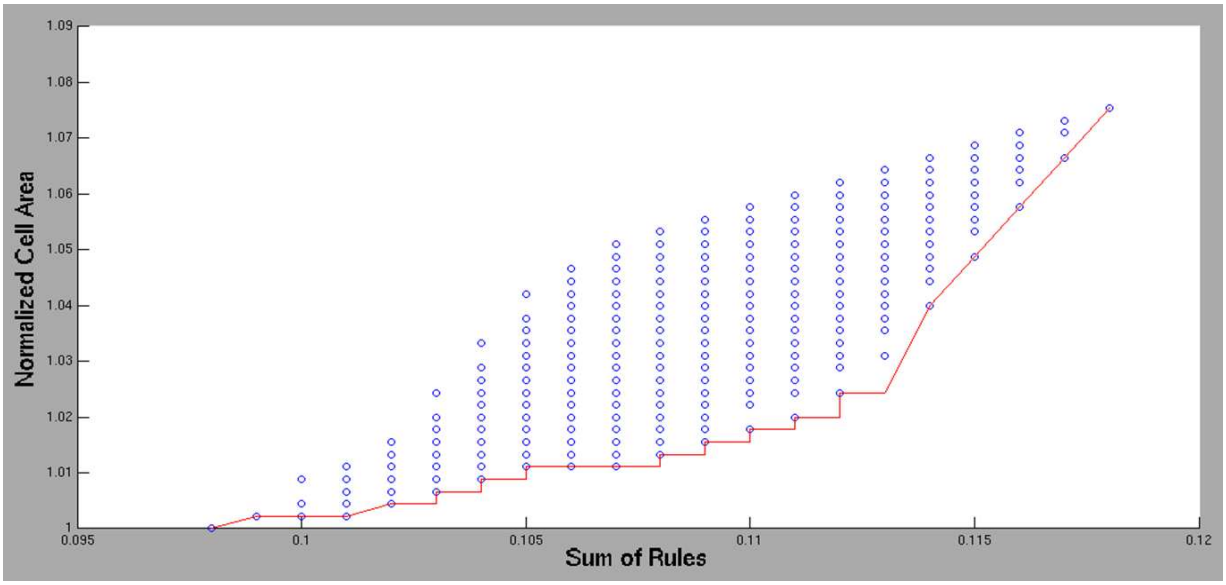

Figure 3. OAI22 cell area versus sum of 3 area-critical DRs.

Table 2. Summary of Boolean minimization for Metal1 layer DR analysis of 20nm standard cell layouts

Cell Name	# Critical Rules	Max. Area Increase (%)	# Multi-level Experiments Required
CKBF2	1	0.6%	17
NAND2	0	0.0%	0
NOR2	1	0.3%	17
MUX21	1	0.6%	17
MUX22	1	0.8%	17
OAI22	0	0.0%	0
SDFFQ	8	1.6%	103181503

4.2 Metal1 DR Analysis

Similar to our analysis method for MOL design rules, 9 Metal1 DRs are analyzed here. Since this layer is double patterned, we focus primarily on different spacing rules, especially those related to line-end, in our analysis. These DRs are typically considered very critical for ensuring native conflict-free layouts without incurring an area penalty. A total of 512 variant layouts are generated in the two-level experiment, which is followed by Boolean minimization. The results after this step are summarized in Table 2. Note that without our experiment reduction approach, a total of 2×10^9 variant layouts need to be generated, since each of the 9 rules that are considered must be varied in steps of $1nm$ between d_i^{min} and d_i^{max}

As we can clearly see from the maximum area increase values in Table 2, Metal1 DRs do not significantly affect the area of any of the standard cells that we analyzed. This behaviour is similar to the results obtained for MOL DRs. This somewhat surprising result indicates that both Metal1 and MOL DRs can be relaxed without any penalty on the area of the standard cell layouts considered here. These result also suggest that polysilicon and active layer DRs are the real limiters for area reduction.

One observation from Table 2 is that for SDFFQ cell layout, the number of variant layouts that need to be generated during the multi-level experiment is very large. This shows that although our method typically provides a significant reduction in experiment count, it does not guarantee a tractable number of variant layouts that must be generated in the multi-level step, as pointed out earlier.

5. CONCLUSIONS AND FUTURE WORK

In this work, we proposed and implemented a novel methodology to simultaneously co-optimize several different design rules using layout compaction to generate layouts by perturbing DR values. We proposed a novel Boolean minimization based approach to reduce the number of layouts that need to be generated via compaction to accurately model standard cell

area as a function of DRs. Our methodology allowed us to automatically discover area-critical DRs and DR interactions, which can potentially help guide rule development during early technology ramp. To demonstrate our methodolody, it is applied to a commercial $20nm$ DR set for MOL and double patterned Metal1 layers. Our results indicate that for most of the standard cell layouts we analyzed, MOL and Metal1 DRs are not area-critical. This suggests that front-end DRs are the area-critical rules that need to be improved in order achieve better scaling.

Although this work focuses on only the area impact of DRs, the methodolody needs to be extended to capture other key metrics that are affected by DR change, especially manufacturing yield. In the future we plan to address this limitation by developing a process metric that can accurately capture the yield of different variant layouts generated through layout compaction. Once area, yield and other relevant metrics are accurately modeled, the goal of automated design rule optimization can be realized.

In addition to developing a process metric to estimate manufacturing yield, approximate experiment reduction methods, which allow further experiment count reduction with only a limited accuracy loss, are being explored.

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