Defect-aware Reticle Floorplanning for EUV Masks

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ABSTRACT

Fabricating defect-free mask blanks remains a major "show-stopper" for adoption of EUV lithography. One promising approach to alleviate this problem is reticle floorplanning with the goal of minimizing the design impact of buried defects. In this work, we propose a simulated annealing based gridded floorplanner for single project reticles that minimizes the design impact of buried defects. Our results show a substantial improvement in mask yield with this approach. For a 40-defect mask, our approach can improve mask yield from 53% to 94%. If additional design information is available, it can be exploited for more accurate yield computation and further improvement in mask yield, up to 99% for a 40-defect mask. These improvements are achieved with a limited area overhead of 0.03% on the exposure field. Defect-aware floorplanning also reduces sensitivity of mask yield to defect dimensions.

1. INTRODUCTION

Extreme ultraviolet(EUV) lithography is considered one of the most promising next generation lithography solutions to replace the current DUV lithography [2]. But the technology still faces several challenges before it can actually be used for volume production. In addition to source and resist, fabricating defect free mask blanks remains one of the major challenges for EUV [16].

A key problem associated with the fabrication of EUV mask blanks, which are essentially multilayer reflecting structures, is buried defects. A sample EUV mask with buried defects is shown in Figure 1. Buried defects are caused due to pits on the substrate surface, or particles that get introduced either on the substrate surface or during multi-layer deposition. Around 75% of defects are caused due to substrate defects. Current technology has enabled mask makers to reduce the density of buried defects down to 0.005 defects/cm^2 for defects larger than 53nm [17]. But detection accuracy of most most inspection tools used today is questionable and actual defect densities are expected to be much higher. Although these defects can be partially repaired using e-beam, there is considerable risk of damaging the multi-layer structure [13]. Because of these issues, it might not be feasible to produce defect-free EUV mask blanks at a reasonable cost.

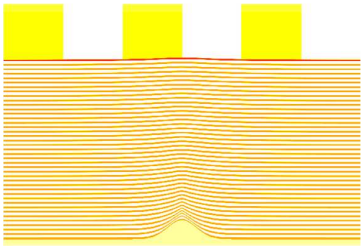


Figure 1. An EUV Mask with buried defects [9].

Due to the challenges associated with producing defect-free EUV blanks, we need to look at methods to print patterns in the presence of these defects. One potential approach to solve this problem is to compensate for the CD impact of these buried defects by modifying the absorber pattern of the design. [8] uses a fast defect printability simulator iteratively to modify the absorber patterns based on thresholded difference between target and simulated images. [7] demonstrates two simple techniques of removing absorber and covering defects with

absorber. Due the fact that buried defects are actually phase defects, compensated layouts are still very sensitive to change in focus and hence have small process window. An alternative method is to move the mask pattern so that defect are avoided. [5] used a simple enumerative technique to move the entire mask pattern so as to avoid buried defects, demonstrating that 70% of designs can be matched to a defective blank. But the method assumes that a defect is harmless if it lies under the absorber. This assumption is inaccurate as the gaussian shape of buried defects means that there can be some design impact of the defect even if most of it lies beneath the absorber. Another observation is that many defects which are not under the absorber may still be harmless either due to non-critical absorber patterns or large distance of defect from any absorber. Their method also entails moving the entire exposure field of the mask away from the center of the blank, which may not be supported by the stepper.

In this work we propose a comprehensive simulated annealing based reticle floorplanning algorithm that can help alleviate the problem of buried defects. Defects are modeled as gaussian shaped and their CD impact is assumed to be proportional to height at edge of the absorber. Assuming that only 1% CD change is acceptable, we can compute the design impact of defects on absorber patterns. Using design impact as a cost metric, we floorplan multiple dies on the mask using a simulated annealing based gridded floorplanner. Design information can be exploited to assign criticality to different design shapes, which can then further improve yield after floorplanning.

This paper is organized as follows. Section 2 discusses the CD impact of buried defects and the model we use to estimate CD impact during floorplanning. Section 3 gives the formal problem definition and then discusses the algorithm for solving the problem. Experimental Results are covered in Section 4 and section 5 concludes this paper.

2. MODELING CD IMPACT OF BURIED DEFECTS

Although CD impact of buried defects has been extensively studied through experiments and simulations [11,18] for different defect dimensions and optical conditions, the focus has always been on dense parallel line patterns. In this work, we assume that similar results will hold for general layout patterns. We use a simple pessimistic linear model for critical dimension (CD) impact of buried defects that was proposed by Clifford et. al [10]. We use the same image slope and fitting constants. In addition to this, we make the following assumptions:

- All defects have a gaussian shape as shown in Figure 2. This assumption is reasonable due to smoothing process during multi-layer deposition [10]. As shown in Figure 2, H is the maximum height of the gaussian defect and full width half maximum (FWHM) is the width of the defect where height is $H/2$.
- CD impact of a defect on a particular absorber is proportional to height of the defect at the closest edge of the absorber. There are two potential sources of error with this assumption. One potential issue is shown in Figure 3(a) below, where our assumption implies that defects D1 and D2 have the same CD impact. In reality, intensity drop of aerial image would be more when most of the defect is not covered by the absorber. The second source of error is due to shadowing due to which the maximum CD change location of a defect is not symmetric.
- To account for defocus, which can have a significant impact on CD [11,18], we scale up the values obtained from the linear model by 3X as a pessimistic approximation based on simulation results from [12], for defocus value of $\pm 75nm$.
- A single absorber pattern cannot be affected by more than one defect. This assumption is reasonable considering the fact that typically defects are randomly distributed across an entire $104mm \times 132mm$ exposure field. Unless defect density is very high, two defects are unlikely to lie close to a single absorber pattern as shown in Figure 3(b).

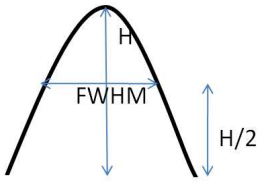
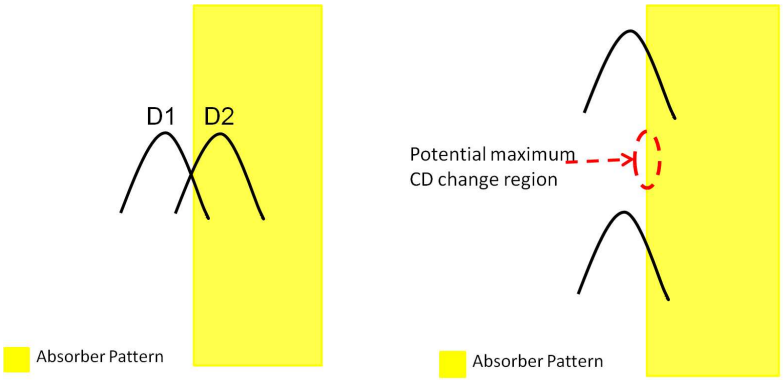


Figure 2. A gaussian defect with height H and full width at half maximum FWHM.



(a) Two potential locations of a defect, D1 and D2 relative to absorber edge. We assume both to have same CD impact but D1 typically has greater CD impact

(b) A scenario with two defects changing CD of a single absorber. The worst case CD change may not lie at minimum distance edge fragement of either defect.

Figure 3. Illustrating some assumptions for modeling of CD impact of buried defect .

With these assumptions, the CD impact for a buried defect as shown in figure 4 can be calculated as:

$$DefectHeight = e^{-r^2/(FWHM/2)^2} \tag{1}$$

$$CD_{defect} = \frac{3 \times \sqrt{I_{NoDefect}}(m_{defect} DefectHeight + b_{defect})}{ImageSlope} \tag{2}$$

where $I_{NoDefect}$, m_{defect}, b_{defect} and $ImageSlope$ are constants whose values are taken from [10] *.

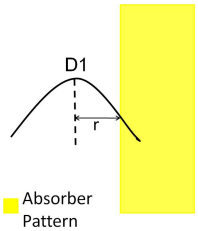


Figure 4. A defect and absorber with r as distance between center of defect and closest absorber edge.

To find out whether a buried defect will cause the design to fail or not, we also need to know the acceptable CD deviation that each design shape can tolerate. This CD tolerance can be computed using the method proposed in [14] if some design information is available to the mask manufacturers. If not, a single conservative

*$m_{defect} = 0.191nm^{-1}, b_{defect} = 0.094, I_{NoDefect} = 0.3$ and $ImageSlope = 0.0471nm^{-1}$

CD tolerance can be assigned to each shape in the design. Using CD tolerance assignment and CD impact of each buried defect, we propose a simple cost metric that estimates the overall design impact of buried defects as,

$$Cost = \sum_{i \in D} \sum_{d \in BD} \sum_{s \in S} e^{CD_{defect}(i,d,s) - CD_{tol}(i,s)} \quad (3)$$

where D is the set of die on the mask, BD is the set of buried defects and S is the set of absorber shapes in the design.

Note that this cost metric is not equivalent to yield but it is indicative of overall electrical impact of buried defects on the design. For example, if a single die has multiple defects, moving the die may not improve yield at all but it could still reduce this cost metric. Another important point is that although we have used a closed form expression to calculate CD impact of a buried defect, it is possible to use a fast simulator such as RADICAL [11] for layout snippets around each buried defect to evaluate the design impact more accurately.

3. DEFECT-AWARE RETICLE FLOORPLANNING

3.1 Problem Formulation

The reticle floorplanning problem for defective EUV mask blanks can be formally stated as follows:

Given a die of dimensions $L_d \times W_d$ with the maximum tolerable CD change of each design shape, and a reticle of dimensions $L_r \times W_r$ along with location and size of buried defects on it, find a reticle floorplan such that the cost function in Eqn. (3) is minimized.

Floorplanning of dies on a mask is an extremely well studied problem in DUV lithography. Most approaches focus on multi-project reticle with dies of different dimensions. The earliest works focused on achieving the most compact placement of rectangles in a given area [6]. B*-tree is an efficient data structure to solve the compact floorplan problem [20]. Many later approaches looked at maximizing the number of chips after dicing the wafer. Kahng et al [15] solved this problem using quadrisection based simulated annealing. The problem was solved as a mixed-ILP in [19].

In this work, we focus on single project reticles and the objective of floorplanning is to maximize yield in the presence of buried defects. We solve the problem for only a single physical layer assuming that all other layers lie on defect-free mask blanks (or are patterned using DUV).

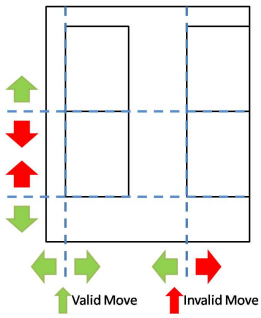
3.2 Problem Solution

To solve the single project reticle floorplanning problem formulated above, we consider only gridded solutions since they guarantee that no die is lost after side-to-side wafer dicing. A non-gridded solution can potentially be more compact but will usually lose some dies during dicing which need to be accounted for during yield computation. We use simulated annealing to solve this optimization problem since previous work on floorplanning suggests that it is a good heuristic for floorplanning problems. In this technique an initial solution is randomly chosen. Any perturbation or change in that solution increases or decreases that cost. If a change or move reduces the cost it is accepted else it is accepted with a finite probability depending on the increase in cost and number of prior iterations. A temperature is usually used as a parameter for this in analogy to thermal annealing. So, initially when the system is hot, most moves, even those that increase cost, are accepted. As the system cools down, the optimizer behaves like a greedy algorithm.

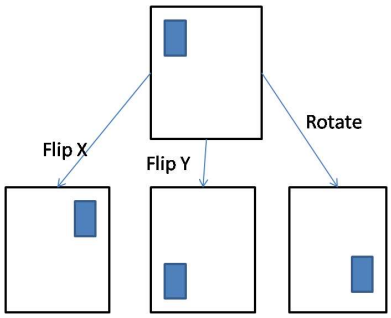
Since we are looking for gridded solutions, we define a set of horizontal and vertical gridlines. If we have an initial compact floorplan with n_r rows and n_c columns of dies, then we have n_r horizontal gridlines and n_c vertical gridlines. Each horizontal(vertical) gridline has it's corresponding y(x) coordinate linked to all die whose bottom (left) coordinate is the same. So, each die is linked to two gridlines, one vertical and one horizontal. Both horizontal and vertical gridlines are sorted by the coordinate of the gridlines. Each gridline coordinate (and all the linked dies) can be increased or decreased by a predefined value, say δ. This is a move or perturbation. Hence a vertical(horizontal) gridline L_i^V (L_i^H) has two possible moves:(1) $x_i(y_i) = x_i(y_i) + \delta$;(2) $x_i(y_i) = x_i(y_i) - \delta$. A move can be valid or invalid based on whether spatial constraints are obeyed after the move is made. The spatial constraints that must be obeyed by every gridline are:

1. $x_0(y_0) > 0.0$
2. $x_i(y_i) - x_{i-1}(y_{i-1}) >= W_d(H_d)$
3. $x_k(y_k) <= W_d(H_d) + W_r(H_r)$

where k is the total number of vertical(horizontal) gridlines, $W_r(H_r)$ is reticle width (height), $W_d(H_d)$ is die width (height) and $i \in 1, 2...k-1$. Figure 5(a) graphically illustrates this definition of moves and their validity. Apart from moving the dies, their orientation can also be changed. Each die can have four possible orientations as shown in Figure 5(b). 90^0 rotation is not considered since it will typically not be allowed due to lithographic patterning constraints. But these orientation changes can have significant manufacturing overheads. Flipping the die would lead to dies with different pin locations and hence require a different package. Rotation by 180^0 makes wafer testing significantly harder (potentially requiring a different probe-card). Due to these overheads, we have disallowed any orientation changes in our algorithm.



(a) Illustration of valid and invalid moves



(b) Illustration of various orientations for a die

Algorithm 1 Reticle Floorplanning Algorithm for EUV Mask

Require: Width (W_d) and Height (H_d) of reticle, width(W_r) and height (H_r) of die, CD tolerance of design shapes and location of defects on mask blank.

Ensure: Location of die such that number of defects in critical areas is minimized.

1: Define $n_c = W_d/W_r$ vertical gridlines starting from origin with spacing W_r.
2: Define $n_r = H_d/H_r$ horizontal gridlines starting from origin with spacing H_r.
3: Place $n_c \times n_r$ dies on the reticle such that each die is linked to one vertical and one horizontal gridline based on bottom left co-ordinate.
4: $T = T_{initial}$, r is cooling rate
5: **while** $T > T_{final}$ **do**
6: Randomly pick one valid move m^* that satisfies spatial constraints.
7: **if** cost(m^*) $<= 0$ **then**
8: Accept m^*.
9: **end if**
10: **if** cost(m^*) > 0 **then**
11: Accept m_{min} with probability $P = exp(-cost(m^*)/T)$.
12: **end if**
13: $T = T * r$.
14: **end while**

Algorithm 1 describes the algorithm. Line 1-3 define an initial partition where dies are placed in a compact

grid on the reticle along with the gridline datastructure. Line 4-5 and 13 define the standard SA iterations. A valid move is chosen and accepted/rejected based on conventional SA criteria in Lines 6-12.

4. EXPERIMENTAL RESULTS

4.1 Setup

For our experiments, we chose buried defects of height, $H = 2nm$ and width, $FWHM = 100nm$ which are randomly distributed over the maximum reticle field area of $104mmX132mm$ [†]. A typical mask blank is larger than the field size and there is some flexibility in choosing the size and location of the exposure field. But in this work, we assume the field is always centered as is typically the case. All results are reported as an average of 1000 random defect distributions. We consider masks as brightfield with GDS shapes corresponding to absorbers. This is a reasonable assumption for poly layer, which is our focus in this work. The schedule for simulated annealing was taken as $T_{initial} = 100000$, $r = 0.99$ and $T_{final} = 0.001$. When making moves, the distance $\delta = 0.5um$. The implementation was done in C++ using OpenAccess API [4].

We perform floorplanning with three different die sizes which are shown in Table 1 along with number of dies that can be fit inside the maximum exposure field area. All three benchmark designs are constructed by tiling copies of the poly layer of a 45nm Mips design, which was placed and routed with 75% utilization in Cadence SoC Encounter [1] using Nangate 45nm library [3]. The 45nm design is scaled down to 22nm before tiling. We then slightly change the exposure field area so that in each case 99.97% of the exposure field is occupied by the design pattern. The exact value of the field size for each die is also mentioned in Table 1.

Table 1. Different die sizes considered

Design Label	Die Size($mm \times mm$)	# Die/reticle	Exposure field($mm \times mm$)
Design A	51.85×65.77	4	103.7×131.5
Design B	51.85×43.85	6	103.7×131.5
Design C	34.45×32.71	12	103.3×130.8

4.2 Impact of design information

In the absence of any design information, the mask maker can assign a fixed CD tolerance to each absorber shape and then use that to perform floorplanning. In this work, we assign a conservative CD tolerance of $0.25nm$, which is 1% of the transistor gate length in a $22nm$ design (wafer scale). The results with this design-unaware approach is shown with different number of defects in Table 2. The proposed cost function before and after the floorplanning along with die yield (*Average percentage of dies per mask for which CD impact of defect is less than CD tolerance*) and mask yield (*Average percentage of masks with all die functioning*) are shown along with average runtime. Mask yield is typically the most important metric for mask makers as it strongly affects manufacturing cost of masks. We can see that mask yield can be improved to around 90% for up to 60 defects for all three dies. The results indicate that die size does not have a significant impact on initial mask yield or the results of floorplanning optimization.

If mask makers are provided with some design information, they can exploit it to assign different CD tolerances to different absorber shapes based on their criticality. One approach to do this has been discussed in [14]. We implement the same method for assigning CD tolerances in this work. Assigning CD tolerances based on criticality reduces the pessimism in yield computation caused by assigning a single CD tolerance to each shape. This can be clearly seen if we compare the initial mask yield of Table 3 compared to Table 2. Design awareness also allows the floorplanner more opportunities to improve yield by placing non-critical absorber edges close to buried defects. The post-floorplanning mask yields of Table 2 and Table 3 illustrate this. For example, with 40 defects, mask yield of reticle with Die B can be improved only up to 94.2% without any design information but it can be improved up to 98.4% with design awareness. The difference in yield is even bigger for larger defect count.

[†]All dimensions in this section are mask scale unless explicitly stated

Table 2. Experimental Results for Reticle Floorplanning without Design Information

Design Label	# Defects	Initial			Final		
		Cost	Die Yield(%)	Mask Yield(%)	Cost	Die Yield(%)	Mask Yield(%)
Design A	20	3038.7	92.7	73	19.2	99.6	98.4
	40	5754.8	86.5	53.3	34.61	98.3	93.7
	60	9045.69	81.2	37.4	72.10	97.0	89.6
	80	11120.1	77.8	31.2	110.58	93.9	80.8
	100	13761.3	72.3	19.5	234.51	91.3	71.8
Design B	20	3038.7	95.1	73	18.59	99.8	98.6
	40	5754.81	90.3	53.3	32.75	98.9	94.2
	60	9045.69	86.8	37.4	126.75	98.0	90.0
	80	11120.1	83.8	31.2	217.4	96.1	82.1
	100	13761.3	79.2	19.5	319.4	94.4	74.2
Design C	20	2648.05	97.7	75.0	18.45	99.9	98.7
	40	5104.3	95.5	56.7	35.42	99.5	94.9
	60	7984.69	93.7	41.7	150.26	99.1	91.5
	80	9872.4	92.2	35.4	128.60	98.3	84.8
	100	12418.1	89.9	22.7	300.35	97.6	78.0

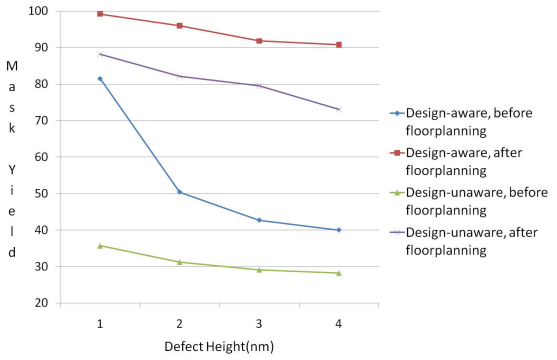
Table 3. Experimental Results for Reticle Floorplanning with Design Information

Design Label	# Defects	Initial			Final		
		Cost	Die Yield(%)	Mask Yield(%)	Cost	Die Yield(%)	Mask Yield(%)
Design A	20	95.52	95.5	82.9	0.03	99.9	99.8
	40	214.49	917	69.2	0.39	99.8	99.2
	60	302.94	87.9	57.3	0.91	99.3	97.5
	80	324.31	85.6	50.4	2.33	98.9	95.8
	100	451.14	81.4	39.3	7.43	98.2	93.3
Design B	20	97.34	97.0	82.9	0.03	99.9	99.8
	40	214.49	94.3	69.2	0.17	99.8	99.1
	60	302.94	91.7	57.3	0.74	99.6	97.7
	80	324.31	89.8	50.4	1.42	99.3	96.0
	100	451.14	86.5	39.3	4.44	98.9	93.9
Design C	20	56.04	98.62	84.4	0.19	99.9	99.7
	40	200.055	97.4	71.8	0.39	99.9	99.1
	60	292.79	96.1	60.8	0.75	99.8	97.9
	80	273.5	95.3	54.5	1.25	99.7	97.0
	100	411.24	93.7	42.8	5.45	99.4	93.4

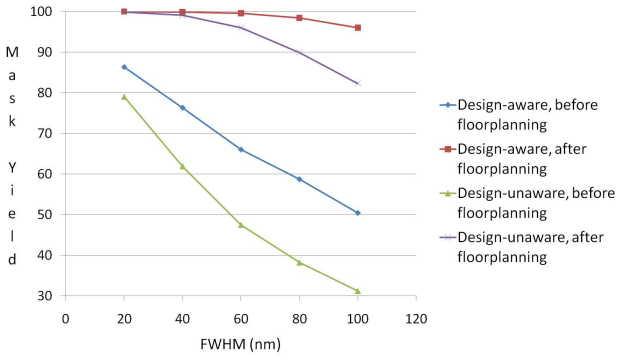
4.3 Impact of defect dimensions

In this section we explore the impact of defect size on mask yield before and after floorplanning. All results in this section correspond to design B with a defect count of 80. We first study the impact of defect height on mask yield. Figure 5(c) shows a plot of mask yield for four different defect heights of 1nm, 2nm, 3nm and 4nm. It shows that design-aware yield decreases exponentially as defect height increases before floorplanning. After floorplanning the impact of defect height is less severe and there is only a small linear decrease in yield. For the design-unaware case, yield before and after floorplanning shows a linear dependence, but has a larger slope compared to when design information is included in the floorplanning.

Figure 5(d) shows mask yield before and after floorplanning for $2nm$ buried defects with FWHM ranging from $20nm$ to $100nm$. The plot shows the strong dependence of mask yield on defect width before floorplanning. This dependence is considerably weakened post-floorplanning as the floorplanner is able to achieve yield above 95% even for $100nm$ wide defects. The figure also shows the benefit of design-aware floorplanning, where dependence of yield on FWHM is almost negligible.



(c) Mask Yield before and after floorplanning for different defect height



(d) Mask Yield before and after floorplanning for different defect widths

Figure 5. Mask Yield for different defect dimensions

These two plots demonstrate the strong sensitivity of mask yield to defect dimensions. This problem can be alleviated by our floorplanner since it takes defect dimensions into account while computing design impact of defects.

4.4 Impact of available free area

Allowing empty space on the exposure field allows more flexibility in placing dies so as to avoid buried defects but it comes at a price. The wasted space reduces the number of dies per wafer. Hence, we need to evaluate how much free space is really required in the exposure field in order to achieve an acceptable mask yield. To perform this experiment we pick Die B and slightly modify the dimensions of the exposure field in order to change the free space. The results for a few cases of design B with defect height of $2nm$ and FWHM of $100nm$ are shown in Figure 6. This shows that our floorplanner can achieve almost 100% yield with a small area overhead of less than 0.01%. The plot also demonstrates that design-awareness and lower defect density helps reduce the area overhead of this approach.

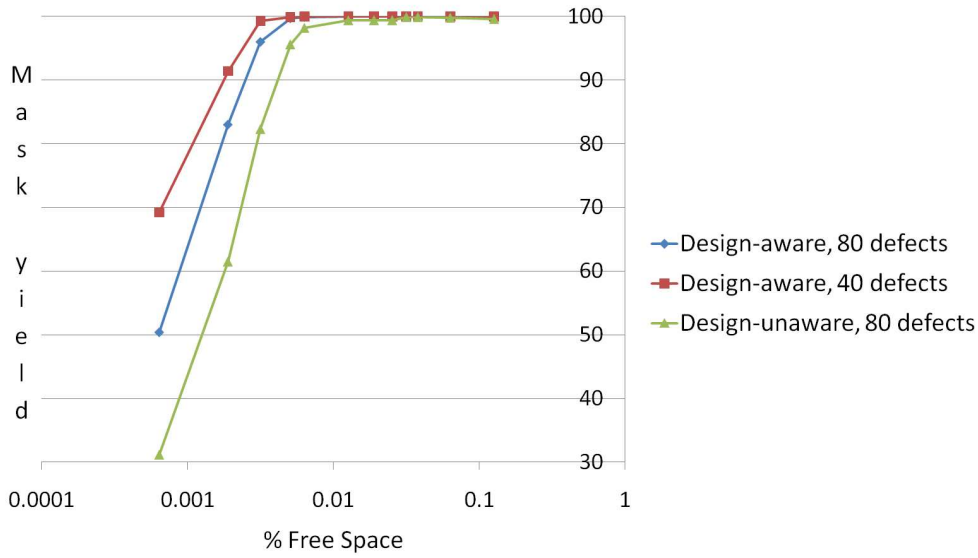


Figure 6. Improvement in post-floorplanning mask yield with free space

4.5 Allowing orientation change

In section 3.2, we briefly discussed the additional overheads of allowing orientation change during floorplanning. But allowing this degree of freedom can have a significant improvement in mask yield, especially at higher defect densities or design-unaware floorplanning, where post-floorplanning yield is low. Table 4 shows the additional improvement with the additional degrees of freedom. The improvement looks small only due to the fact that post-floorplanning yield is higher than 95% for all the shown cases, even without the additional degrees of freedom. But the results demonstrate potential improvements from this additional flexibility, which can be utilized to reduce the area overhead, which would improve the number of chips per wafer.

Table 4. Mask yield for different orientations

Design Type	Defects	Final Mask Yield (%)		
		No Orientation change	Only 180^o	All allowed
Design B, design-unaware	80	82.3	88.8	99.2
Design B, design-unaware	60	90	93.3	99.5
Design B, design-aware	80	96	96.6	100

5. CONCLUSION AND FUTURE WORK

In this work, we proposed a simulated annealing based reticle floorplanner that minimizes the design impact of buried defects on EUV mask blanks. We propose a simple model to estimate the CD impact of gaussian shaped buried defects in the presence of absorber patterns, based on existing literature on EUV defect simulations. We proposed an algorithm for floorplanning single project masks in a gridded fashion which improves mask yield substantially, from around 53% to 94% for a 40-defect mask. Adding design information, which essentially allows assigning different CD tolerances to different shapes, can result in further improvements in mask yield, up to 99% for a 40-defect mask. This improvement was achieved with a limited area overhead on the exposure field of only 0.03%. Our floorplanning approach also reduces the sensitivity of mask yield to defect dimensions. Allowing change in orientation of dies, which can have a significant overhead, allows us to reduce the exposure area even further.

One key assumption of most works dealing with defective masks, including ours is that inspection tools can accurately locate the position and shape of buried defects on the blank. Most current inspection tools are unable to do this. Making the floorplanning solution more robust to error in exact defect location is one useful improvement that we wish to explore in the future. We would also like to solve the floorplanning problem when multiple phsyical layers of the design are patterned on defective blanks. Physical layer to mask blank mapping is an important part of the multi-layer problem which we are looking into. Our current model for CD impact of buried defects is inaccurate. We wish to incorporate a fast image simulator for EUV masks to predict CD impact more accurately. Generalizing the floorplanner to deal with multi-project reticles and come up with non-gridded floorplans, which take dicing yield into account is also worth exploring in the future.

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